Matrox Solios eV

Installation and Hardware Reference

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Chapter 1

Introduction

This chapter briefly describes the features of the Matrox Solios eV-CL boards, as well as the software that can be used with the boards.

Matrox Solios eV-CL boards

The Matrox Solios eV-CL boards are high-performance Camera Link frame grabbers. There are two versions available: a PCIe dual-Base/single-Medium version and a PCIe single-Medium/single-Full version. These are referred to as Matrox Solios eV-CLB and eV-CLF, respectively. Each version is also available with the same auxiliary connectors as the original Matrox Solios eCL board. These are referred to as Matrox Solios eV-CLBL and eV-CLFL, respectively.

To change the configuration of Matrox Solios eV-CL from its factory-default setting of single-Medium to dual-Base, use MILConfig (Solios tab) and follow all on-screen instructions. Once changed, you must restart your computer (perform a cold-boot) for changes to take effect.

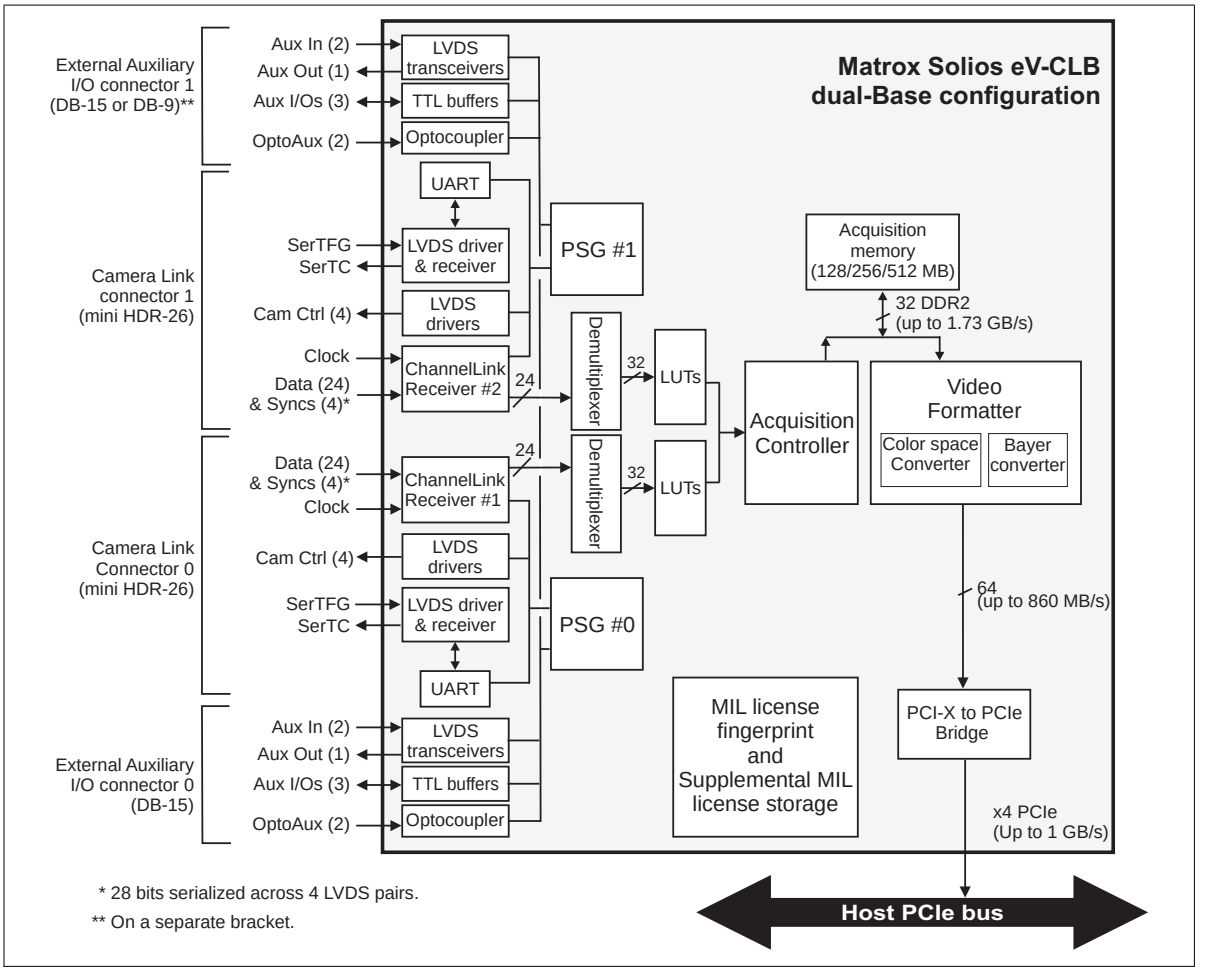
❖ The PCIe single-Medium/single-Full board is capable of operating in either configuration without any changes.

This manual uses the term Solios eV-CL to refer to Matrox Solios eV-CLB, Matrox Solios eV-CLBL, Matrox Solios eV-CLF, and Matrox Solios eV-CLFL. When necessary, this manual distinguishes between the boards using their full names.

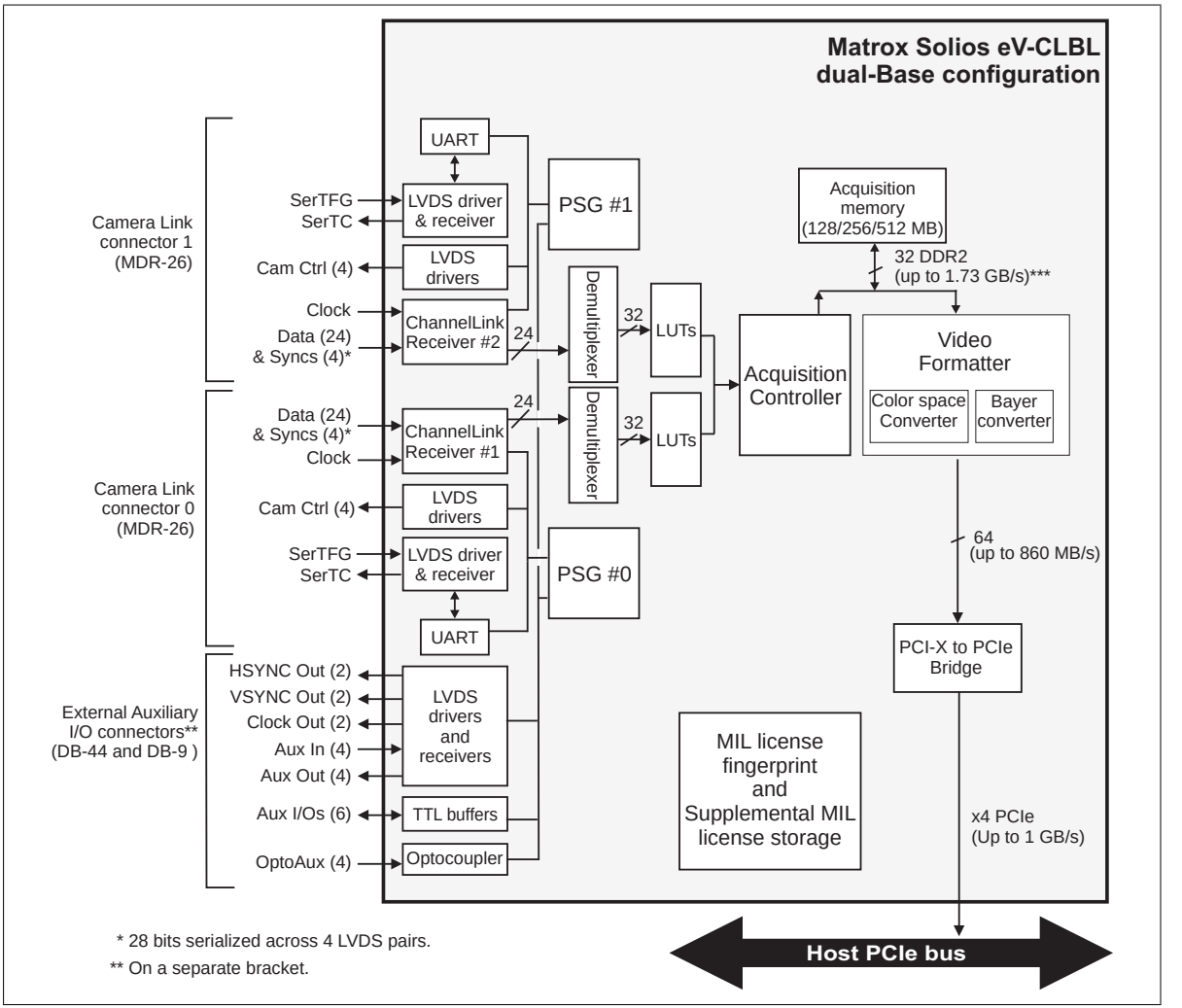
Matrox Solios eV-CLB and eV-CLBL

When in dual-Base configuration, Matrox Solios eV-CLB and eV-CLBL support acquisition from up to two Camera Link devices. When in single-Medium configuration, the boards support one Camera Link device. Matrox Solios eV-CLB and eV-CLBL support power-over Camera Link (PoCL) connections. Matrox Solios eV-CLB and eV-CLBL support Camera Link frequencies of up to 85 MHz.

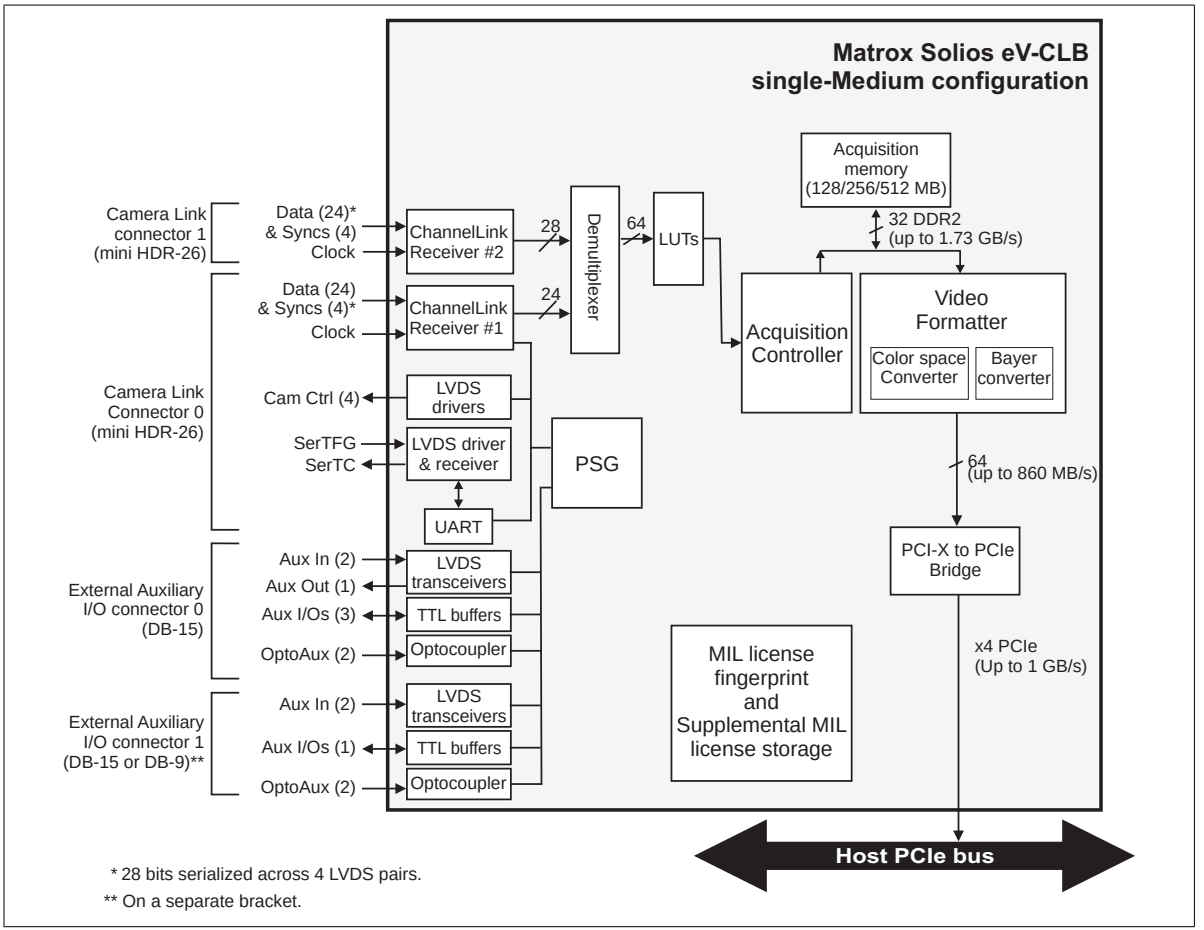
The following flow diagram shows Matrox Solios eV-CLB in dual-Base configuration.



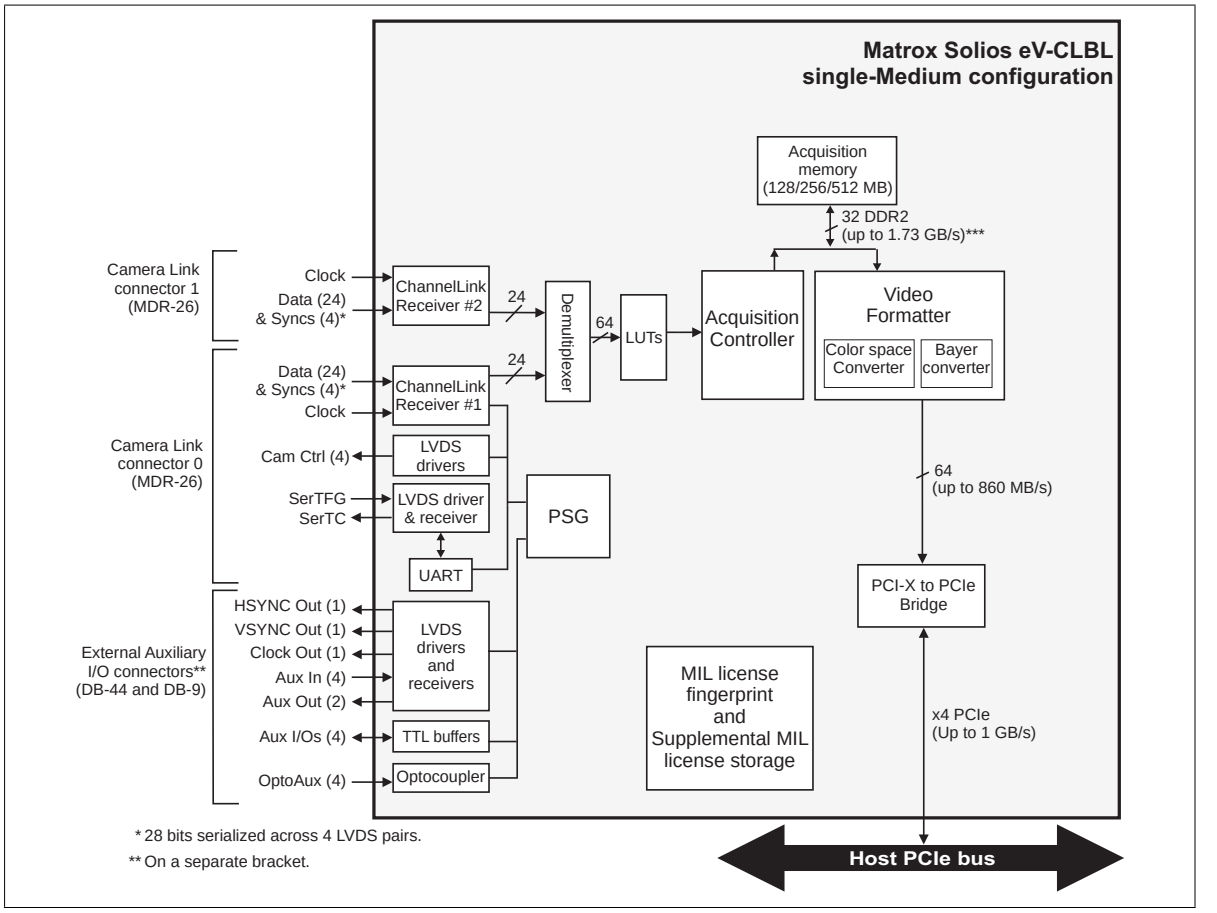
The following flow diagram shows Matrox Solios eV-CLBL in dual-Base configuration.



The following flow diagram shows Matrox Solios eV-CLB in single-Medium configuration.



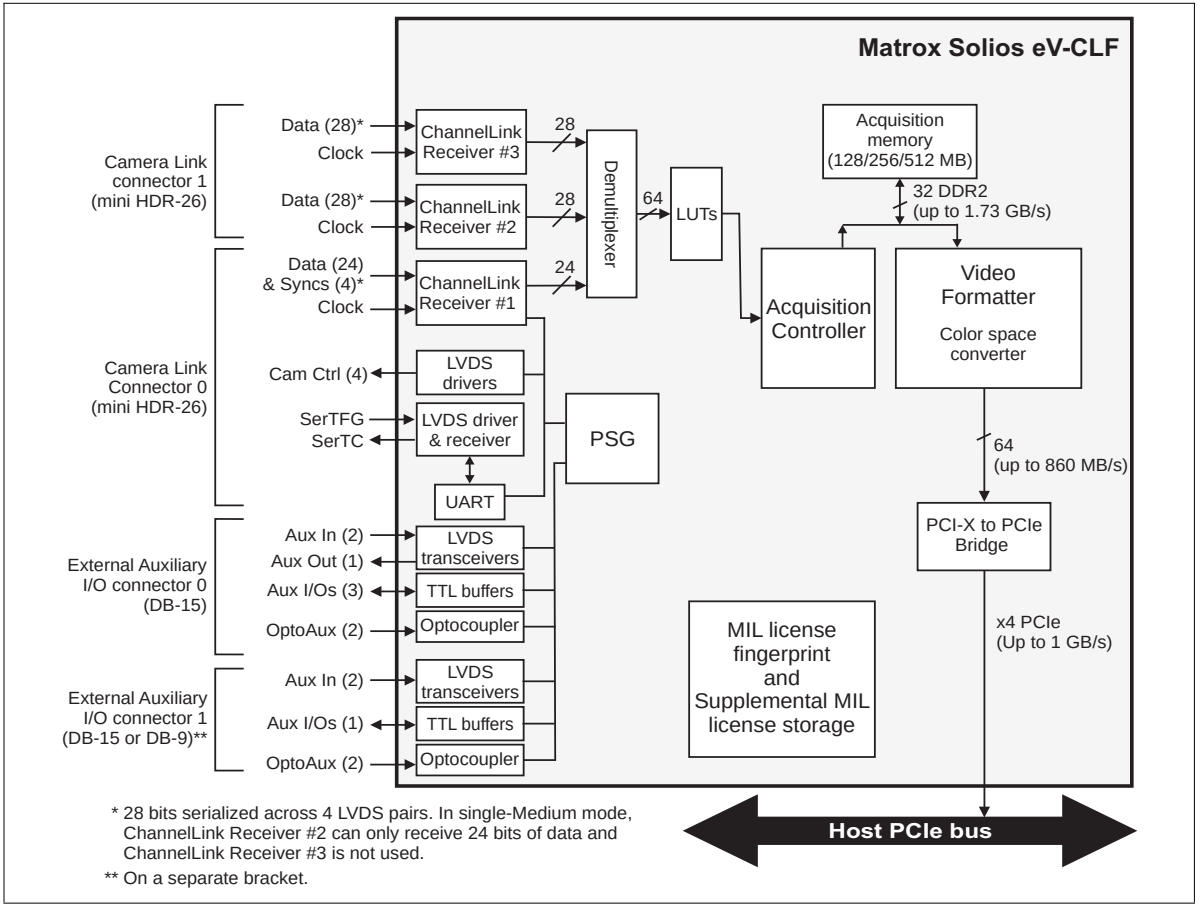
The following flow diagram shows Matrox Solios eV-CLBL in single-Medium configuration.



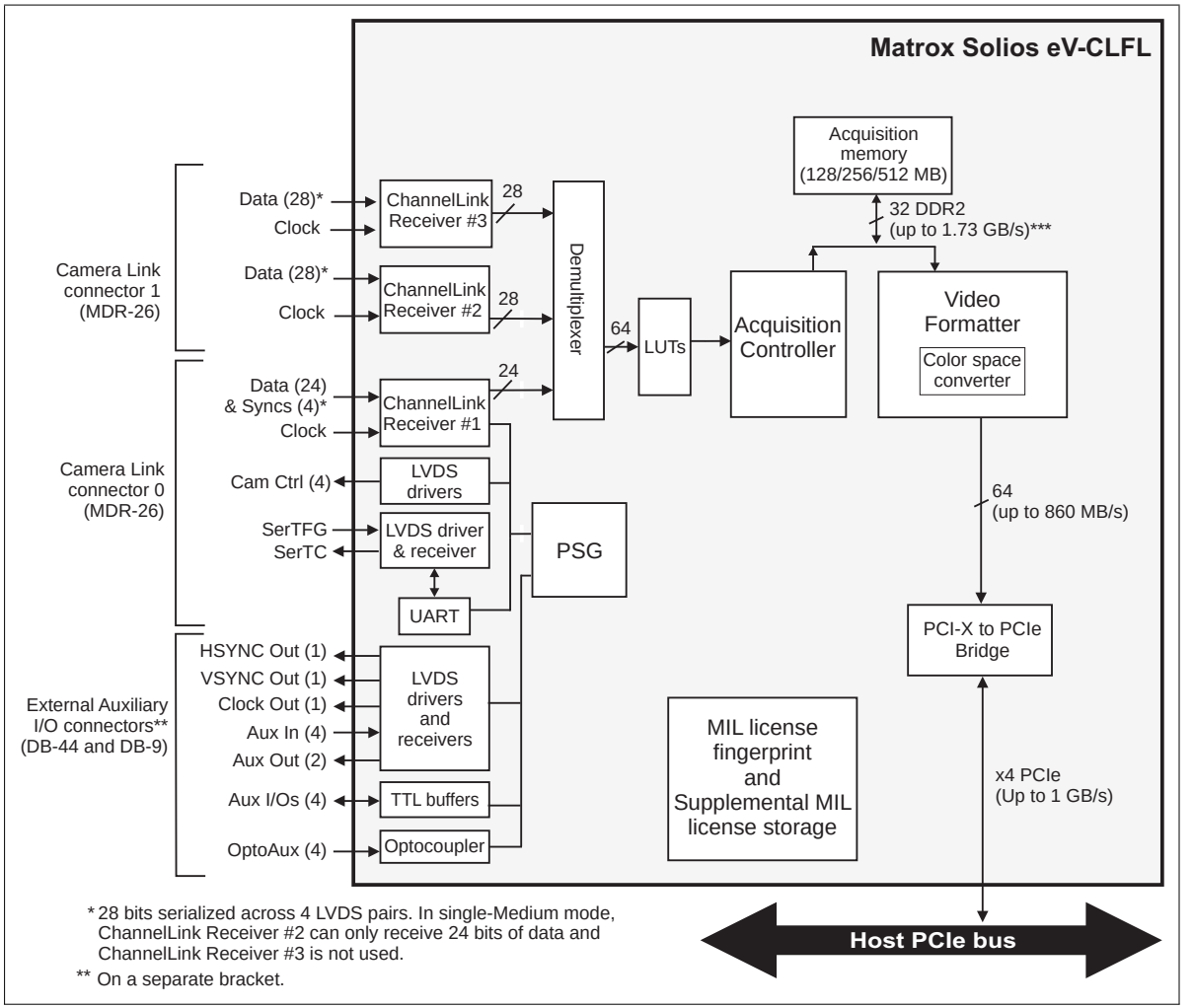
Matrox Solios eV-CLF

Matrox Solios eV-CLF and eV-CLFL support acquisition from one Camera Link device in single-Medium or single-Full configuration (with up to 10 taps). Matrox Solios eV-CLF and eV-CLFL support Camera Link frequencies of up to 85 MHz. Note that when using a 10 tap 8-bit video source, the maximum Camera Link frequency is 70 MHz when grabbing to Host and 80 MHz when grabbing on-board.

The following flow diagram shows Matrox Solios eV-CLF in single-Medium and single-Full configuration.



The following flow diagram shows Matrox Solios eV-CLFL in single-Medium and single-Full configuration.



* 28 bits serialized across 4 LVDS pairs. In single-Medium mode, ChannelLink Receiver #2 can only receive 24 bits of data and ChannelLink Receiver #3 is not used.

** On a separate bracket.

General acquisition features

Matrox Solios eV-CL supports area and line-scan monochrome and color video sources. The color video sources can be RGB video sources or video sources with a Bayer color filter. Matrox Solios eV-CLB and eV-CLBL can decode the color information of Bayer color-encoded images; whereas, Matrox Solios eV-CLF and eV-CLFL can only transfer the images to the host computer (Host) for decoding. Besides standard Camera Link video sources, Matrox Solios eV-CL also supports additional types of video sources, including time-multiplexed video sources.

On-board memory

Matrox Solios eV-CL supports 128, 256, or 512 Mbytes of linearly addressable 32-bit 216 MHz DDR2 SDRAM to store acquisition data. This memory is referred to as acquisition memory.

Additional functionality

In addition to the core video capture capabilities, Matrox Solios eV-CL incorporates a variety of features to simplify overall system integration. These features include:

- LVDS-compatible serial interfaces (2 for Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration, 1 for Matrox Solios eV-CLB and eV-CLBL in single-Medium configuration, and 1 for Matrox Solios eV-CLF and eV-CLFL). Each interface is mapped as a COM/ttyS port so that it can be accessed through the operating system communication API. The serial interface can both receive and transmit signals, in full-duplex mode.

- Color space converter. The converter allows captured data to be converted to RGB24, RGB32, or YUV16 format. In addition, data can be converted to 8-bit, 10-bit, 12-bit, 14-bit and 16-bit monochrome data.

- Auxiliary, multi-purpose signals, which can be configured as user-defined signals, or to some other functionality depending on the auxiliary signal (for example, as trigger input, field polarity input, timer-clock input, or exposure output signals). The number of signals each board supports is given in the table below.

Board	Auxiliary signals available
Matrox Solios eV-CLB	16*
Matrox Solios eV-CLBL	18†
Matrox Solios eV-CLF	13*
Matrox Solios eV-CLFL	14†

. This is the number of auxiliary signals available when using the DB-15 auxiliary I/O connector on the cable adapter bracket; if replaced with the optional DB-9 connector from the SOLEVAACC01PAK accessory kit, fewer auxiliary signals are available (see the pinout of the auxiliary I/O connector in *Appendix B: Technical information*).

†. This is the number of auxiliary signals available when using both the DB-9 and DB-44 auxiliary I/O connectors on the cable adapter bracket.

- Integrated quadrature decoders (2 for Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration, 1 for Matrox Solios eV-CLB and eV-CLBL in single-Medium configuration, and 1 for Matrox Solios eV-CLF and eV-CLFL). These can decode input from a rotary encoder with quadrature output.

Data transfer

Under optimum conditions, Matrox Solios eV-CL can exchange data with the Host at a peak transfer rate of up to 1 Gbyte/sec; the maximum achievable bandwidth depends on the type of camera and digitizer configuration format (DCF) used. Optimum conditions include using the board in a PCIe slot with 4 active lanes.

Although the Matrox Solios eV-CL boards do not have an integrated display section, images can be transferred either to any available Matrox display board or a third-party display board in the computer.

Important

Note that transfer of image data to a display board might require intervention from the Host CPU, depending on your computer's architecture.

Software

To operate Matrox Solios eV-CL, you can use one or more Matrox Imaging software products that support the board. These are the Matrox Imaging Library (MIL) and its derivatives (MIL-Lite, ActiveMIL, ActiveMIL-Lite, Matrox Inspector, and Matrox Intellicam). All Matrox software is supported under Windows; MIL is also supported under Linux when using Matrox Solios eV-CL. Consult your software manual for supported versions of these operating systems.

MIL

MIL is a high-level programming library with an extensive set of optimized functions for image capture, processing, analysis, transfer, compression, display, and archiving. Image processing operations include point-to-point, statistical, spatial filtering, morphological, geometric transformation, and FFT operations. Analysis operations support calibration, are performed with sub-pixel accuracy, and include pattern recognition (normalized grayscale correlation and Geometric Model Finder), blob analysis, edge extraction and analysis, measurement, image registration, metrology, character recognition (template-based and feature-based), code recognition and verification (1D, 2D and composite code types), bead inspection (continuous strip of material), 3D reconstruction, and color analysis.

MIL applications are easily ported to new Matrox hardware platforms and can be designed to take advantage of multi-processing and multi-threading environments.

MIL-Lite

MIL-Lite is a subset of MIL. It includes all the MIL functions for image acquisition, transfer, display control, and archiving. It also allows you to perform processing operations that are typically useful to pre-process grabbed images.

ActiveMIL

ActiveMIL is a set of ActiveX controls that are based on MIL. ActiveMIL was designed for rapid application development (RAD) tools, such as Microsoft's Visual Basic.Net. ActiveMIL is included with MIL (ActiveMIL-Lite is included with MIL-Lite).

Matrox Inspector

Matrox Inspector is an interactive Windows application for image capture, processing, analysis, and archiving. Matrox Inspector is included with MIL. MIL application developers can use Matrox Inspector as a prototyping tool to quickly build proof-of-concept demonstrations. End users can use Matrox Inspector to perform and automate image enhancement and measurement tasks.

Matrox Intellicam

Matrox Intellicam is an interactive Windows program that allows for fast video source interfacing and provides interactive access to all the acquisition features of your Matrox board. Matrox Intellicam also has the ability to create custom digitizer configuration format (DCF) files, which MIL and its derivatives use to interface to specific non-standard video sources. Matrox Intellicam is included with all Matrox Imaging software products.

Essentials to get started

To begin using Matrox Solios eV-CL, you must have a computer with the following:

- An available conventional x4 (or better) PCIe slot.
- Processor with an Intel 32-bit architecture (IA32) or equivalent.
- A relatively up-to-date PCIe chipset. The list of platforms that are known to be compatible with Matrox Solios eV-CL are available on the Matrox website, under the board's PC compatibility list.
- MIL or one of its derivatives. This software should be installed after you install your board.

Consult your software package for other computer requirements (for example, operating system and memory requirements).

Inspecting the Matrox Solios eV-CL package

You should check the contents of your Matrox Solios eV-CL package when you first open it. If something is missing or damaged, contact your Matrox representative.

Standard items

You should receive the following:

- The Matrox Solios eV-CLB, eV-CLBL, eV-CLF, or eV-CLFL board, depending on which was purchased

- Depending on the board purchased, you will receive a different alternative cable adapter bracket to access the signals of the internal auxiliary I/O connectors from outside the computer enclosure.

  - With the Matrox Solios eV-CLB and Matrox Solios eV-CLF you should receive a cable adapter bracket with one DB-15 connector.

  - With the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL you should receive a cable adapter bracket with either two DB-15 connectors or one DB-44 and one DB-9 connectors, depending on which cable adapter bracket you chose.

Available separately

You might have also ordered one or more of the following:

- MIL, which includes ActiveMIL and Matrox Inspector; MIL-Lite, which includes ActiveMIL-Lite. Matrox Intellicam is included with each of the aforementioned software packages.

- SOLEVAACC01PAK* accessory kit. This kit is only for use with Matrox Solios eV-CLB and eV-CLF; it is not for use with Matrox Solios eV-CLBL and eV-CLFL. The accessory kit has an alternative cable adapter bracket to access the signals of the internal auxiliary I/O connectors from outside the computer enclosure. This bracket has a DB-9 connector instead of a DB-15 auxiliary I/O connector. The DB-9 connector has the same pinout as auxiliary I/O connector 1 (DB-9) on the adapter board of the original Matrox Solios eCL/XCL board. Note however, when using the DB-9 connector, some DB-15 signals are not available.

❖ If needed, you can purchase a Camera Link or PoCL-compliant Camera Link cable (HDR or SDR) from the video source manufacturer, Components Express inc., 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties.

Handling components

The electronic circuits in your computer and the circuits on Matrox Solios eCL/XCL are sensitive to static electricity and surges. Improper handling can seriously damage the circuits. Be sure to drain static electricity from your body by touching a metal fixture (or ground) before you touch any electronic component. In addition, do not let your clothing come in contact with the circuit boards or components.

Warning

Before you add or remove devices from your computer, always **turn off** the power to your computer and all peripherals.

Installation

The installation procedure consists of the following steps:

1. Complete the hardware installation as described in *Chapter 2: Hardware installation*.

2. Complete the software installation procedure described in the documentation accompanying your software package.

More information

For information on using multiple Matrox Solios eV-CL boards, refer to *Chapter 3: Using multiple Matrox Solios eV-CL boards*.

For in-depth hardware information, refer to *Chapter 4: Matrox Solios eV-CL hardware reference*; whereas for a summary of this information, as well as environmental and electrical specifications, and connector pinout descriptions, see *Appendix B: Technical information*.

This manual occasionally makes reference to a MIL-Lite function. However, anything that can be accomplished with MIL-Lite can also be accomplished with MIL, ActiveMIL, ActiveMIL-Lite, or Matrox Inspector.[1]

Need help?

If you experience problems during installation or while using this product, refer to the support page on the Matrox Imaging web site: www.matrox.com/imaging/support. This page provides answers to frequently asked questions, as well as offers registered customers additional ways of obtaining support.

If your question is not addressed and you are currently registered with the MIL maintenance program, you can contact technical support. To do so, you should first complete and submit the online Technical Support Request Form, accessible from the above-mentioned page. Once the information is submitted, a Matrox support agent will contact you shortly thereafter by email or phone, depending on the problem.

1. Most operations can be accomplished with ActiveMIL, ActiveMIL-Lite, and Matrox Inspector.

Chapter

2

Hardware installation

This chapter explains how to install your Matrox Solios eV-CL board in your computer.

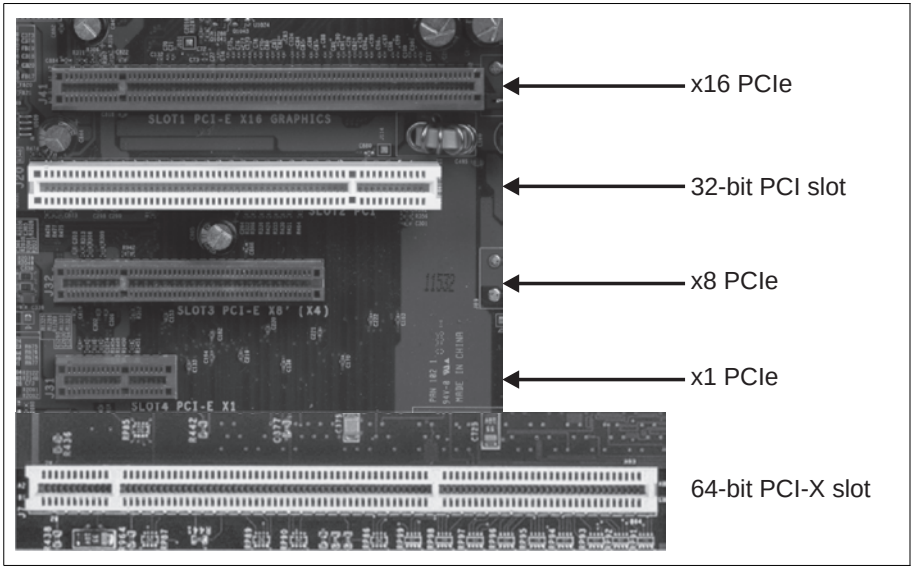
Installing your Matrox Solios eV-CL board

Before you install your Matrox Solios eV-CL board, some precautionary measures must be taken. Turn off the power to your computer and its peripherals, and drain static electricity from your body (by touching a metal part of the computer chassis).

Proceed with the following steps to install your board. Note that your board should be installed before you install your software.

1. Remove the cover from your computer; refer to your computer's documentation for instructions.

2. Check that you have an empty PCIe slot (x4 or better) in which to install your Matrox Solios eV-CL.



Matrox Solios eV-CL might drop frames if there are not at least 4 active lanes on the PCIe connector to the Host (for example, if the board is connected to a x4 PCIe connector that has only one active lane). Verify with your motherboard manufacturer to find out whether your motherboard works efficiently with a x4 PCIe board, such Matrox Solios eV-CL.

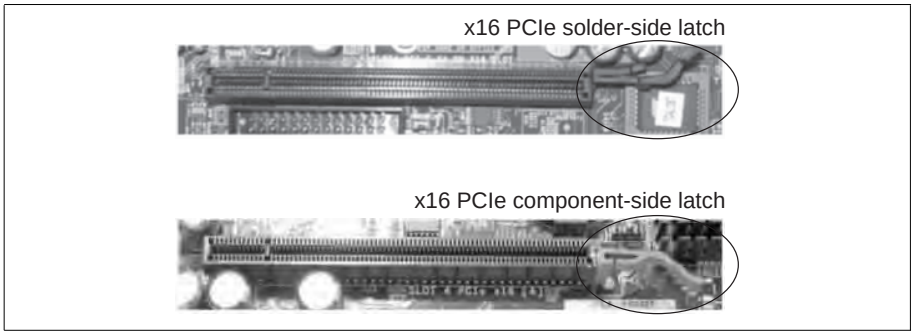
If you also need to install the cable adapter bracket of your Matrox Solios eV-CL board, you need an additional slot. This slot does not need to be adjacent to the Matrox Solios eV-CL board. Note that the cable adapter bracket does not plug into a slot's connector; it attaches only to the back of the computer's chassis.

3. If there is a metal plate at the back of the selected slots, remove it. Keep the screw from the top of the plates to anchor your boards once they are installed.

4. Position your Matrox Solios eV-CL board in the selected slot, and then press the board firmly but carefully into the connector of the slot.

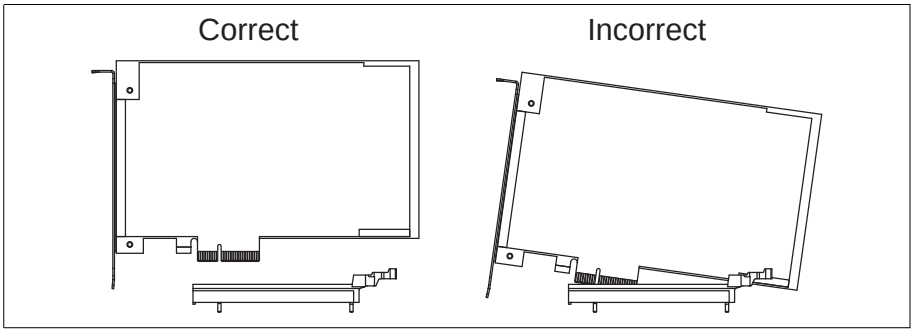
Important

When installing a Matrox Solios eV-CL board in a x16 PCIe slot, special care must be taken to avoid damaging the board. Some x16 PCIe slots have a connector with a retainer. Matrox Solios eV-CL boards ***must not*** come into contact with the latch of this retainer.



The PCIe specification does not define appropriate keep-out regions for the latch to provide any tolerance to tilting or rotation when inserting or removing add-in boards in these connectors. Therefore, do not to tilt the Matrox Solios eV-CL

board backwards or rotate it when installing it; otherwise the board can touch the latch and get damaged. Note that the same is true when removing the board. Alternatively, you can remove the latch from the retainer.



5. Anchor the board using the screw that you removed in step 3.

6. If required, install the cable adapter bracket of your Matrox Solios eV-CL board, as described in the section *Installing the cable adapter bracket*, later in this chapter.

7. Attach your video sources, as described in the section *Connecting video sources*, later in this chapter.

8. Turn on your computer.

❖ When you boot your computer under Windows, Windows' Plug-and-Play system will detect a new Multimedia Video Device and you will be asked to assign it a driver. At this point, you should click on **Cancel**. Under Windows and Linux, the driver will be installed during the installation of Matrox Solios eV-CL software.

9. Disable active state power management (ASPM) for PCIe devices, to maximize the performance of Matrox Solios eV-CL. In the BIOS, disable all ASPM (or equivalent) settings (typically accessible from the **Power management** submenu of the **Advanced Configurations** menu). In addition, if the operating system has an **ASPM for PCIe devices** option, disable this option as well. For example, in Microsoft Windows 7, open the **Power Options** dialog box from the Windows Control Panel. For the currently selected power plan, click on **Change Plan Settings** and then click on **Change Advanced Power Settings**. In the presented dialog, expand **PCI Express**, and then expand **Link State Power Management** and set it to **Off**.

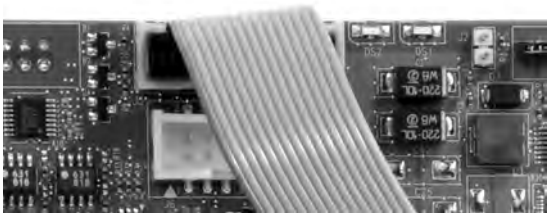
Installing the cable adapter bracket

To install the cable adapter bracket of Matrox Solios eV-CL, proceed with the following steps:

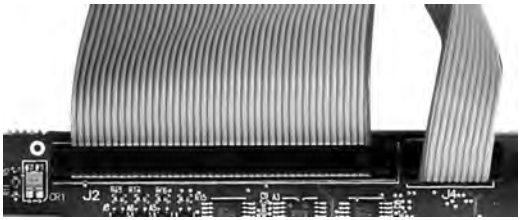
1. Make sure that your Matrox Solios eV-CL board is fastened to the computer chassis.

2. Attach the cable adapter bracket's flat ribbon cable to the appropriate internal auxiliary I/O connector on the Matrox Solios eV-CL board. To attach the flat ribbon cable, position the cable so that the red wire is on the same side as the bracket of the Matrox Solios eV-CL board. With the Matrox Solios eV-CL board and the cable in this position, connect the cable's connector to the appropriate internal auxiliary I/O connector.

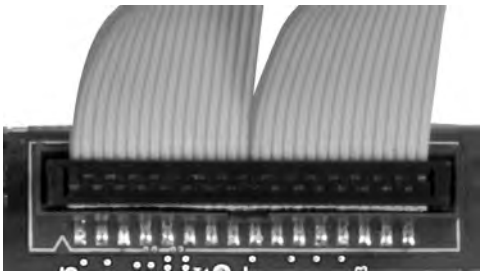
   If you have a single DB-15 connector on your cable adapter bracket, you should attach the flat ribbon cable to the top internal auxiliary I/O connector; whereas if you have a single DB-9 connector on your cable adapter bracket, you should attach the flat ribbon cable to the bottom connector.



If you have DB-44 and DB-9 connectors on your cable adapter bracket, you should attach the flat ribbon cable of the DB-44 connector to the internal auxiliary I/O 44-pin connector and you should attach the flat ribbon cable of the DB-9 connector to the internal auxiliary 10-pin connector.



If you have two DB-15 connectors on your cable adapter bracket, you should attach the flat ribbon cables of the dual DB-15 connectors to the top internal auxiliary I/O 32-pin connector.



3. Slide the bracket into the opening at the back of the selected slot.

4. Anchor the bracket to the chassis using the screw that you removed in the previous section.

Connecting video sources

Connecting to Matrox Solios eV-CLB or Matrox Solios eV-CLF boards

The Matrox Solios eV-CLB and Matrox Solios eV-CLF boards have the following connectors on their bracket:

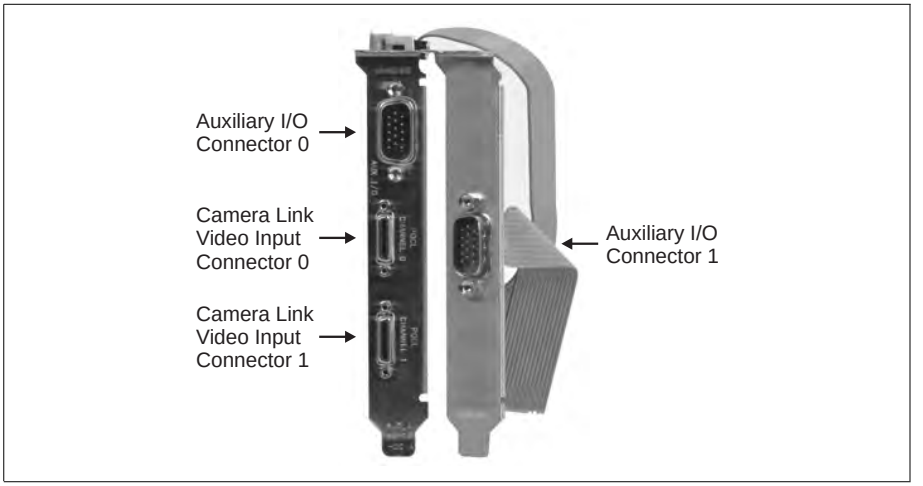
- **Two mini Camera Link-compliant video input connectors.** Used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.

- **External auxiliary I/O connector 0 (DB-15).** Used to transmit/receive auxiliary signals for one of the acquisition paths. By default, it carries the auxiliary signals for acquisition path 0; if a jumper is installed on the 2-pin I/O acquisition path jumper block, the auxiliary I/O connector carries the auxiliary signals for acquisition path 1.

- **Internal auxiliary I/O connectors (16-pin and 10-pin).** Used to transmit/receive auxiliary signals. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

To access the signals of the internal auxiliary I/O connectors, you might have installed the cable adapter bracket. It has the following connector:

- **External auxiliary I/O connector 1 (DB-15 or DB-9).** Used to transmit/receive auxiliary signals for the other acquisition path.



To Matrox Solios eV-CLB in dual-Base configuration, you can connect two independent video sources; one to each Camera Link connector. To Matrox Solios eV-CLB in single-Medium configuration and to Matrox Solios eV-CLF, you can only connect a single video source, regardless of the source's configuration.

Warning

Connecting a single-Medium video source to a board operating in dual-Base configuration could seriously damage your video source. Note that for Matrox Solios eV-CLB, the board is factory configured to operate in single-Medium configuration.

To connect video sources to the Camera Link connectors, use standard Camera Link cables with a 26-pin high-density male mini Camera Link connector (HDR or SDR) at one end. For Matrox Solios eV-CLB, you should use PoCL-compliant Camera Link cables (HDR or SDR) when connecting to PoCL-compliant video sources. Camera Link cables are not available from Matrox; for possible sources, see the *Connectors on Matrox Solios eV-CLB and eV-CLF boards* section in *Appendix B: Technical information*.

❖ If using both Camera Link connectors to connect to the same video source (single-Medium or single-Full configuration), the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

Connecting to Matrox Solios eV-CLBL or eV-CLFL boards

Matrox Solios eV-CLBL and Matrox Solios eV-CLFL boards have the following connectors:

- **Two Camera Link-compliant video input connectors.** Used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.

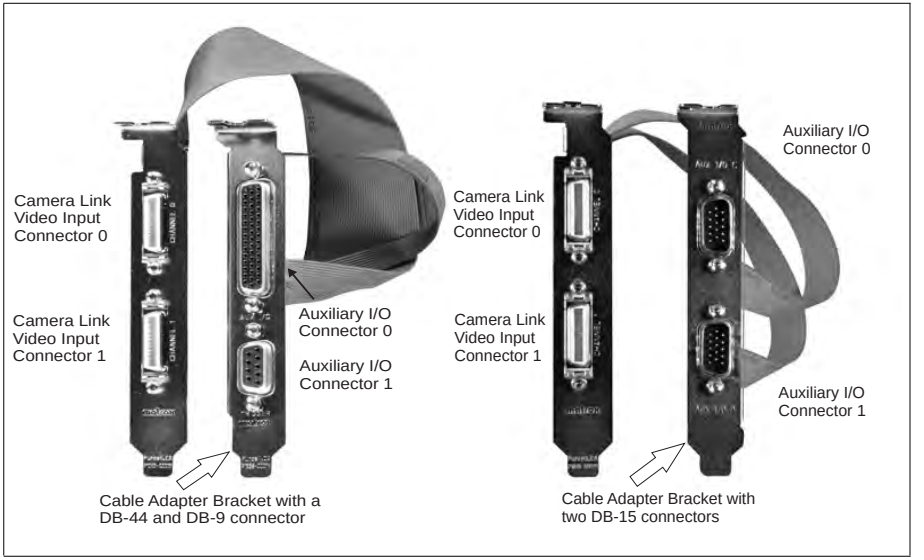
- **Internal auxiliary I/O connectors (44-pin/10-pin or 32-pin).** Used to transmit timing and synchronization signals, and transmit/receive auxiliary signals. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

  Matrox Solios eV-CLBL and Matrox Solios eV-CLFL come with either the 44-pin/10-pin connectors, for use with the DB-44/DB-9 cable adapter bracket, or the 32-pin connector, for use with the dual DB-15 cable adapter bracket.

  To access the signals of the internal auxiliary I/O connector from outside of the computer enclosure, you might have installed the corresponding adapter board. It has the following connectors:

- **External auxiliary I/O connector 0 (DB-44 or top DB-15).** Used to transmit/receive auxiliary signals. Additionally, the DB-44 connector is also used to transmit timing and synchronization signals.

- **External auxiliary I/O connector 1 (DB-9 or bottom DB-15).** Used to transmit/receive auxiliary signals.



To Matrox Solios eV-CLBL in dual-Base configuration, you can connect two independent video sources; one to each Camera Link connector. To Matrox Solios eV-CLBL in single-Medium configuration and to Matrox Solios eV-CLFL, you can only connect a single video source, regardless of the source's configuration.

Warning

Connecting a single-Medium video source to a board operating in dual-Base configuration could seriously damage your video source. Note that for Matrox Solios eV-CLBL, boards are all factory configured to operate in single-Medium configuration.

To connect video sources to the Camera Link connectors, use standard Camera Link cables with a 26-pin high-density male Camera Link connector (MDR) at one end. For Matrox Solios eV-CLBL, you should use PoCL-compliant Camera Link cables (MDR) when connecting to PoCL-compliant video sources. Camera Link cables are not available from Matrox; for possible sources, see the *Connectors on Matrox Solios eV-CLB and eV-CLF boards* section in *Appendix B: Technical information*.

❖ If using both Camera Link connectors to connect to the same video source (single-Medium or single-Full configuration), the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

Chapter

3

Using multiple Matrox Solios eV-CL boards

This chapter explains how to use multiple Matrox Solios eV-CL boards.

Multiple board installation

You can install and use multiple Matrox Solios eV-CL boards in one computer.

Install each additional Matrox Solios eV-CL board as you installed the first board (refer to *Chapter 2: Hardware installation*). Theoretically, you can have as many as 16 Matrox Solios eV-CL boards installed in your computer; however, this number is computer-dependent.

Using MIL-Lite, you have to allocate a MIL system for each board and allocate the resources of each MIL system. For more information, see **MsysAlloc**() in the MIL Reference.

Simultaneous image capture from different boards

You can simultaneously capture images from video sources attached to different Matrox Solios eV-CL boards; however, the number of video sources from which you can simultaneously capture images is computer-dependent.

The use of a high performance PCIe chipset is necessary to sustain PCIe transfers to Host memory. The list of platforms that are known to be compatible with Matrox Solios eV-CL are available on the Matrox web site, under the board's compatibility list.

To measure the effective, available bandwidth of the PCIe interface used by your Matrox Solios eV-CL board, you can use the SoliosBench tool integrated in the MILConfig utility. As a reference point, capturing from a 1K x 1K, 8-bit, 60 frames/sec video source will require a minimum bandwidth of 63 Mbytes/sec, plus an additional bandwidth margin of approximately 20%, for a bandwidth of 75 Mbytes/sec.

Chapter

4

Matrox Solios eV-CL hardware reference

This chapter explains the architecture, features, and modes of the Matrox Solios eV-CL hardware.

Matrox Solios eV-CL hardware reference

This chapter provides information on the Matrox Solios eV-CL hardware. It covers the architecture, features, and modes of their acquisition section. In addition, it covers the Matrox Solios eV-CL hardware related to the transfer of data. A summary of the features of Matrox Solios eV-CL, as well as pin assignments for the various connectors, can be found in *Appendix B: Technical information*.

Acquisition path

This manual uses the term acquisition path to refer to a path that has the components to digitize or capture a video input signal. The term *independent acquisition path* is used to refer to an acquisition path that can, if required, acquire data from an input source independently from another such path on the same frame grabber. Each independent acquisition path has its own programmable synchronization generator (PSG) to manage all video timing, synchronization, triggering, exposure, and user-defined input and output signals for the path.

MIL-Lite uses the concept of a MIL digitizer to represent the acquisition path(s) with which to grab from one input source of the specified type. When several MIL digitizers are allocated, their device number along with their DCF identify if they represent the same path(s) (but perhaps for a different input format) or independent path(s) for simultaneous acquisition. MIL-Lite uses the concept of a data input channel to identify which input source to use when several of its type are connected to the same acquisition path(s) (for example, grab from channel 0 (video source A) or channel 1 (video source B) of digitizer 0).

Digitizer configuration format

To program the acquisition section, allocate a MIL digitizer using **MdigAlloc**() with an appropriate DCF (supplied or created) and digitizer device number; to select the required input channel, use **MdigChannel**(). If you find a DCF file that is suitable for your video source, but you need to adjust some of the more common settings, you can do so directly, without adjusting the file, using the appropriate MIL-Lite function. For more specialized adjustments, use the Matrox Intellicam program to adjust the DCF file. Using Matrox Intellicam, you can set the active video region, the sampling clock, and all the other parameters related to the timing of the video signal (that is, standard and non-standard video, interlaced or non-interlaced) in your DCF file.

Matrox Solios eV-CL acquisition section

Matrox Solios eV-CL can capture video from digital video sources compliant with the Camera Link specification. Matrox Solios eV-CLB and eV-CLBL can provide power over Camera Link (PoCL) to attached video sources.

Matrox Solios eV-CL supports monochrome, RGB color, and Bayer color-encoded acquisition. Matrox Solios eV-CLB and eV-CLBL can decode the color information of Bayer color-encoded images; whereas, Matrox Solios eV-CLF and eV-CLFL can only transfer the images to the Host for decoding. Besides standard Camera Link video sources, Matrox Solios eV-CL supports additional types of video sources, including time-multiplexed video sources.

Using the color space converter of the video formatter, grabbed data can be converted to RGB24, RGB32, or YUV16 format. In addition, data can be converted to 8-bit, 10-bit, 12-bit, 14-bit, and 16-bit monochrome data.

Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration have two independent acquisition paths. Matrox Solios eV-CLB and eV-CLBL, in single-Medium configuration, and Matrox Solios eV-CLF and eV-CLFL have one acquisition path.

Each acquisition path can grab up to 85 Mega-samples/sec.[1] Each acquisition path has its own programmable synchronization generator (PSG), LUTs, and formatters, and can have a different acquisition rate.

Matrox Solios eV-CL supports a comprehensive set of general purpose I/O signals and serial ports to control cameras and other video sources.

1. Note that when using a 10 tap 8-bit video source, the maximum Camera Link frequency is 70 Mega-samples/sec when grabbing to Host and 80 Mega-samples/sec when grabbing on-board.

Performance

The video timing parameters supported by the board are as follows:

	Maximum
Number of pixels / line (including sync and blanking)	64 K
Number of lines / frame (including sync and blanking)	64 K
Pixel clock	85 Mhz
Bandwidth	660 Mbytes/sec*

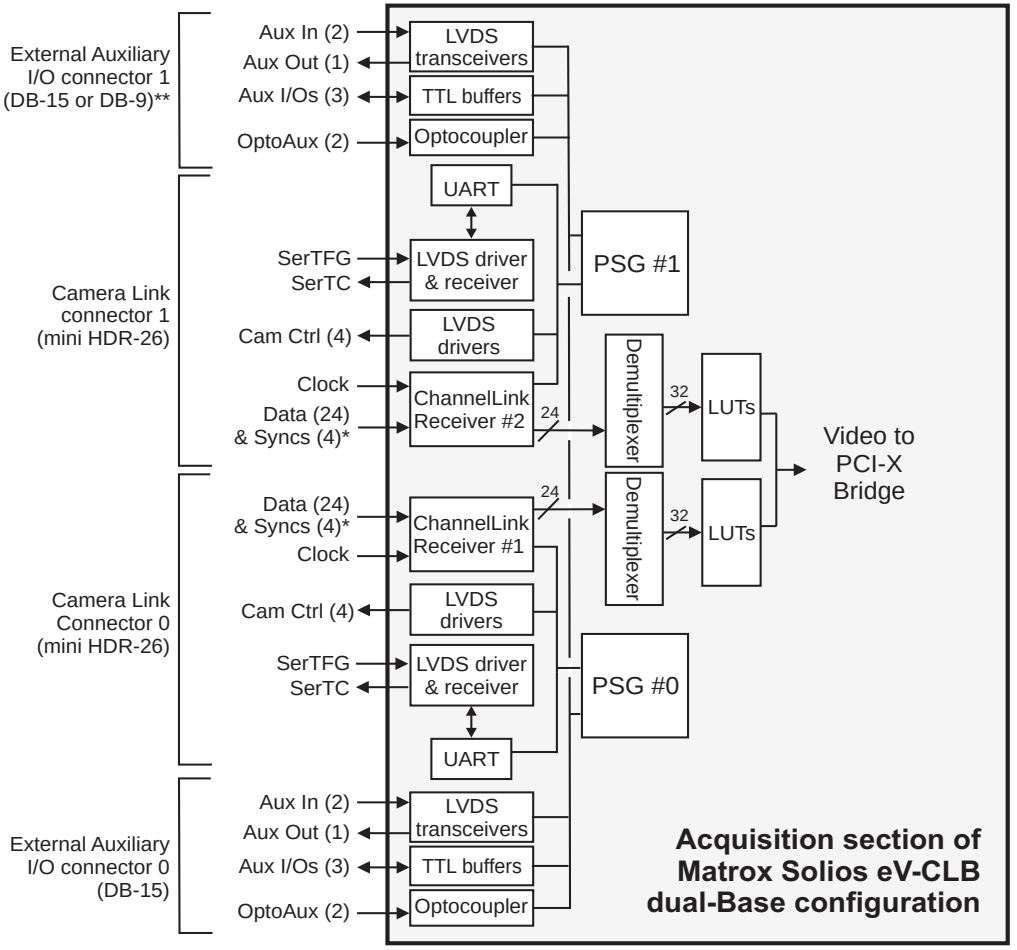
*. Depends on the number of non-consecutive taps.

The maximum pixel clock frequency is dependent on the length of the cable used. Refer to the *Technical features of Matrox Solios eV-CL* subsection of the *Board summary* section in *Appendix B: Technical information*.

Acquisition

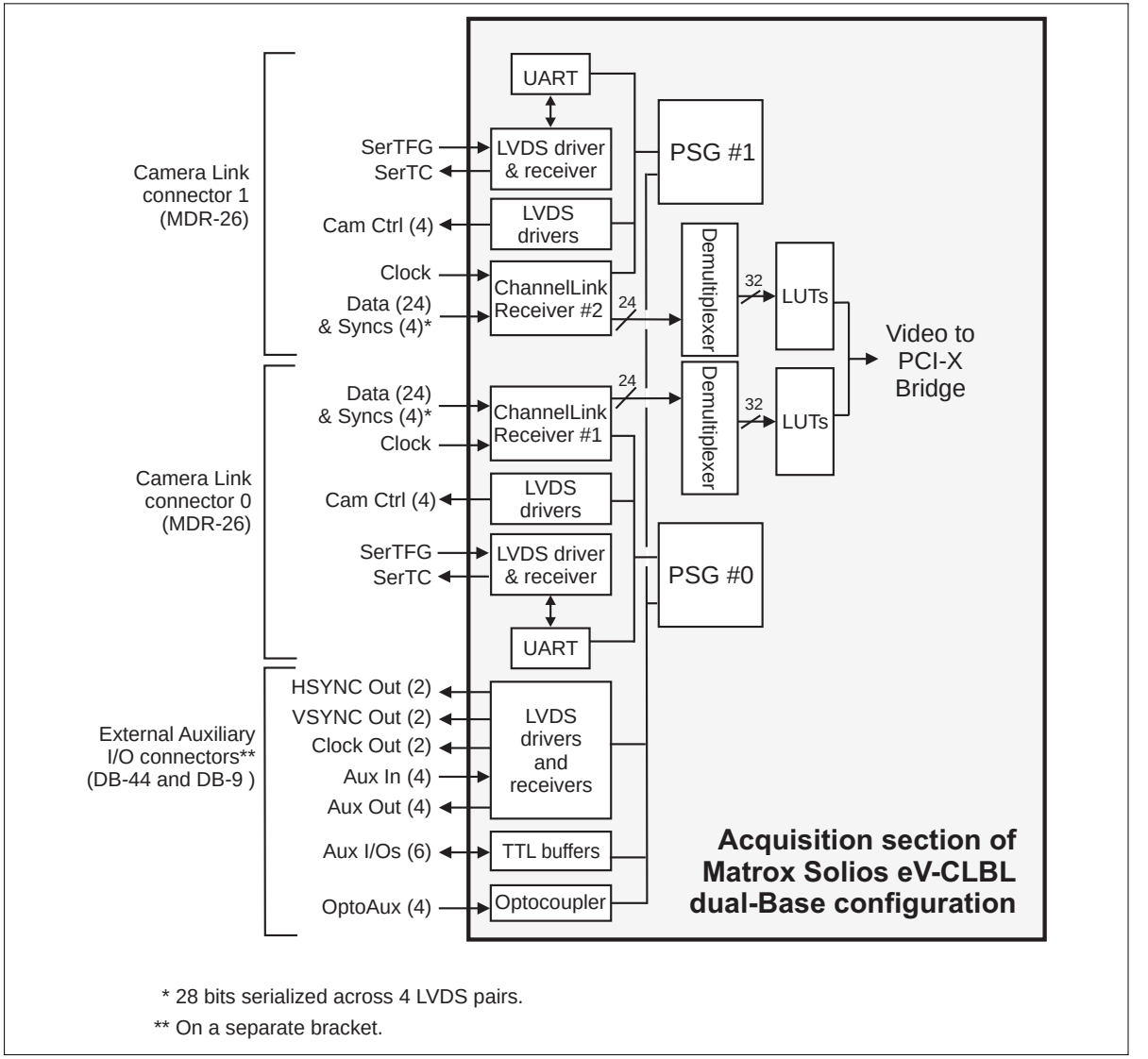
A Base-type acquisition path supports a maximum of 24 bits of video data when acquiring from Camera Link-compliant video sources or up to 32 bits when acquiring from non-standard time-multiplexed video sources. Similarly, a Medium-type acquisition path can grab up to 48 bits of video data when acquiring from Camera Link-compliant sources or up to 64 bits when acquiring from non-standard time-multiplexed sources. Finally, a Full-type acquisition path supports up to 64 bits of video data when acquiring from Camera Link-compliant video sources and up to 80 bits when acquiring from non-standard video sources.

The video sources can be frame, field, or line-scan video sources. Note that the acquisition paths in dual-Base configuration are completely independent, and therefore the video sources do not need to be identical when running in dual-Base configuration.



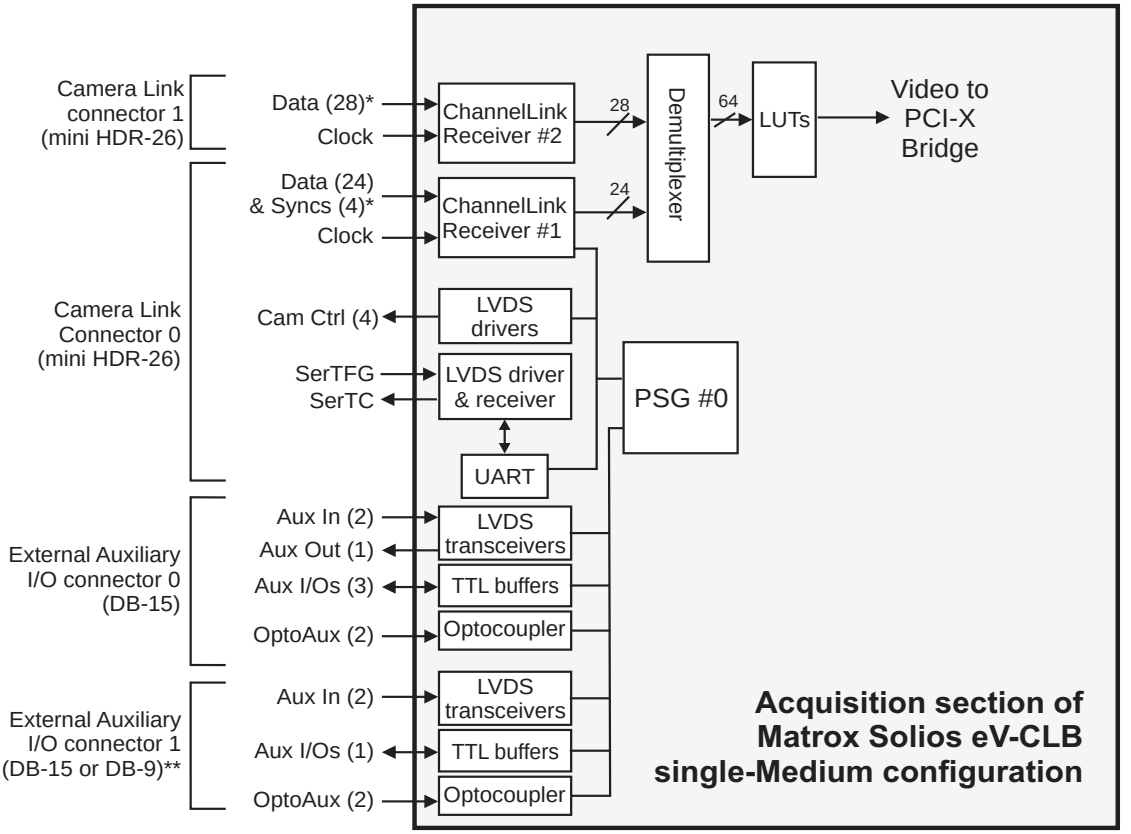
* 28 bits serialized across 4 LVDS pairs.

** On a separate bracket. Note that on a DB-9 connector, not all depicted signals are used.



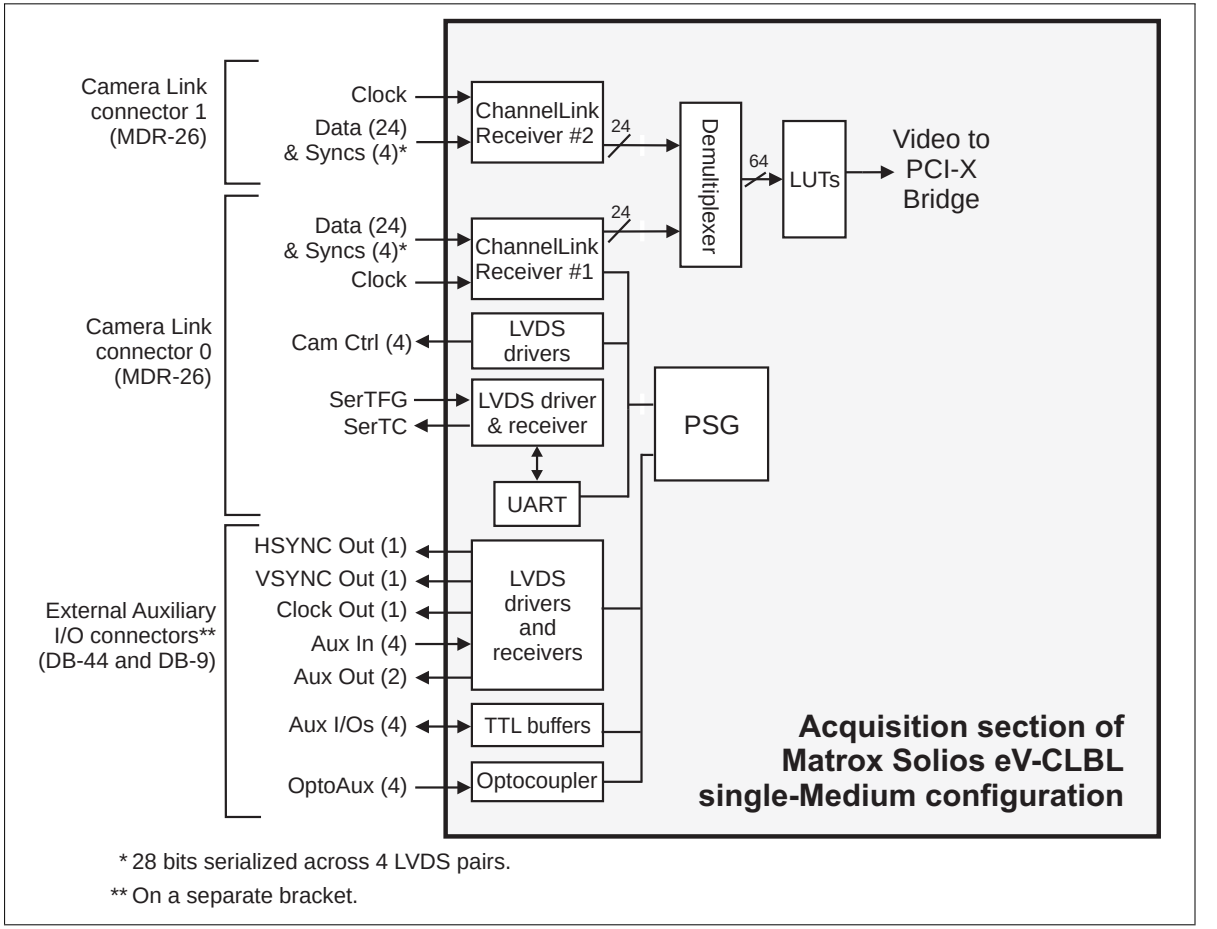
* 28 bits serialized across 4 LVDS pairs.

** On a separate bracket.



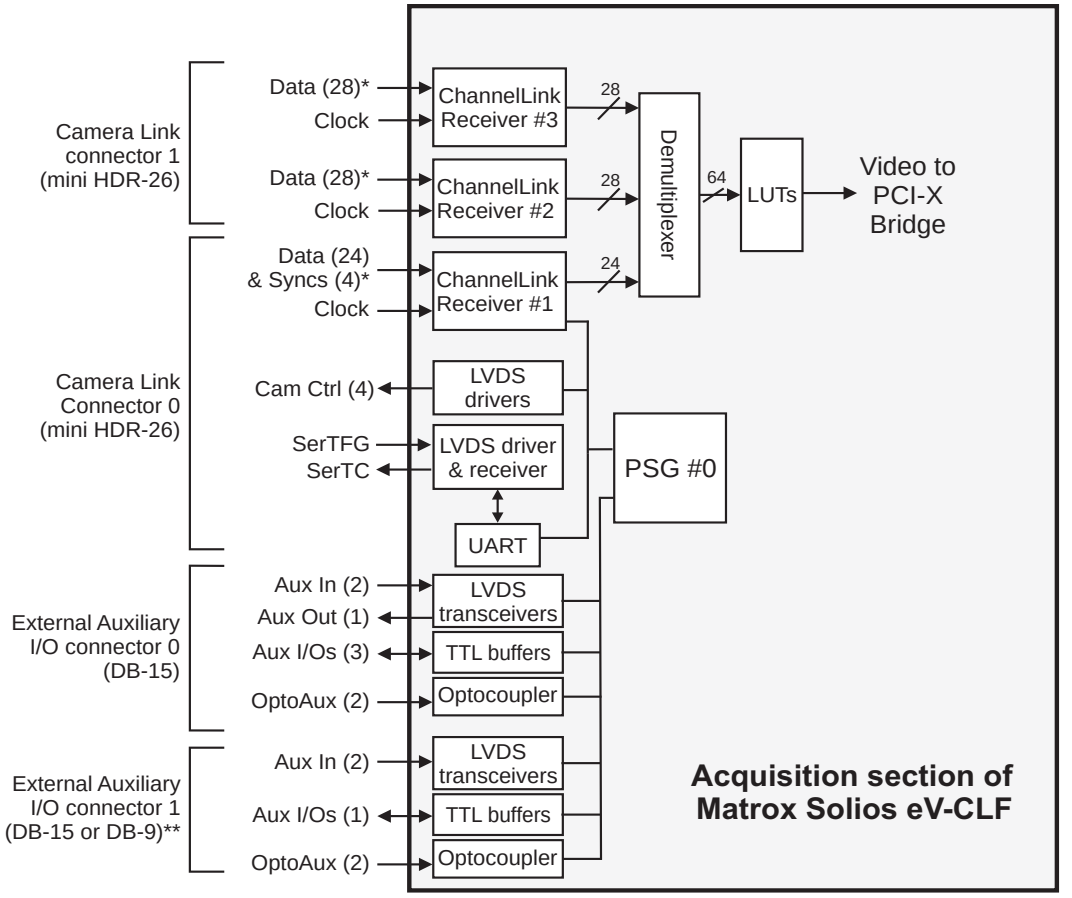
* 28 bits serialized across 4 LVDS pairs.

** On a separate bracket. Note that on a DB-9 connector, not all depicted signals are used.



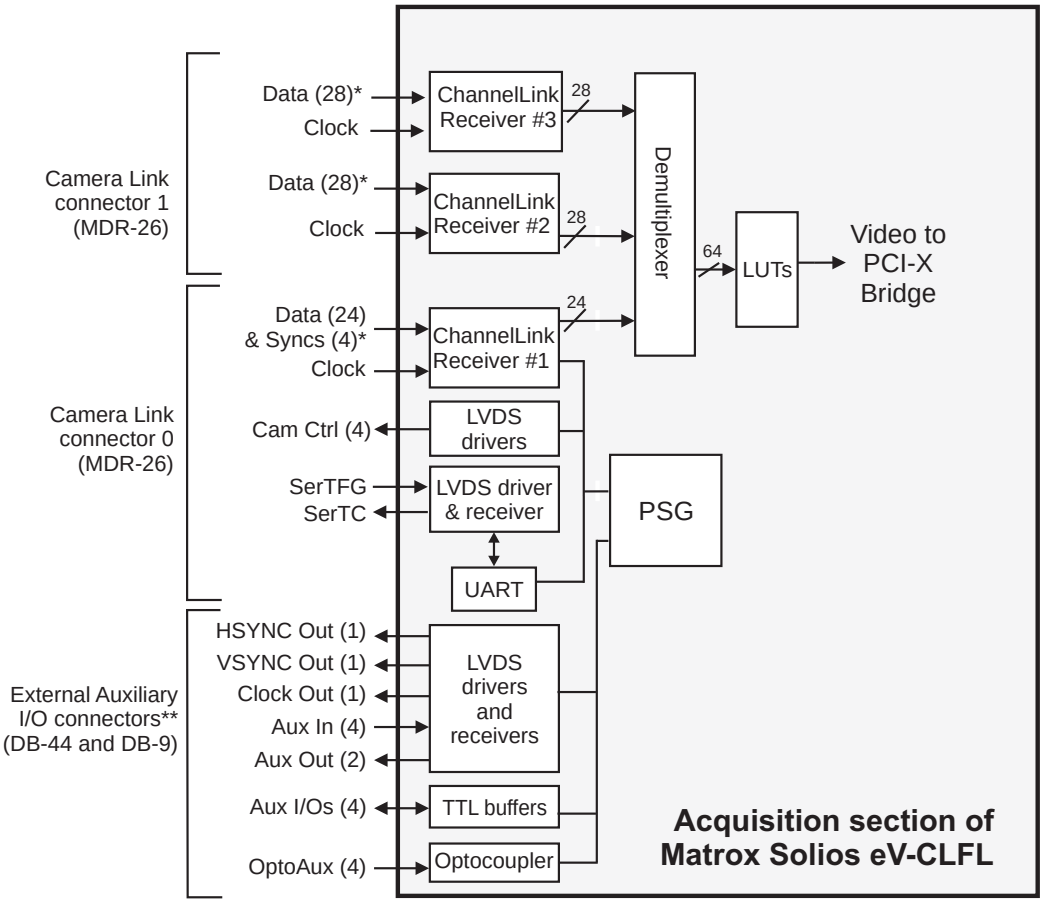
* 28 bits serialized across 4 LVDS pairs.

** On a separate bracket.



* 28 bits serialized across 4 LVDS pairs. In single-Medium mode, ChannelLink Receiver #2 can only receive 24 bits of data and ChannelLink Receiver #3 is not used.

** On a separate bracket. Note that on a DB-9 connector, not all depicted signals are used.



* 28 bits serialized across 4 LVDS pairs. In single-Medium mode, ChannelLink Receiver #2 can only receive 24 bits of data and ChannelLink Receiver #3 is not used.

** On a separate bracket.

Supported video sources

Each acquisition path supports the following video sources:

	Video sources supported per acquisition path
Camera Link Standard	• One tap x 8/10/12/14/16-bit. • Two tap x 8/10/12-bit. • One 3 x 8-bit (RGB). • Four tap 8-bit with time-multiplexing.
Not Camera Link Standard	• Two tap 14/16-bit with time-multiplexing. • Four tap x 10/12-bit with time-multiplexing.

In addition to the above video sources, the following video sources are supported when running in single-Medium configuration:

	Video sources supported
Camera Link Standard	• Four tap x 8/10/12-bit. • One 3 x 10/12-bit (RGB).
Not Camera Link Standard	• 8 tap x 8-bit with time-multiplexing (using only 2 receivers). • Two tap x 14/16-bit. • One 3 x 14/16-bit (RGB). • Two 3 x 8-bit (RGB) (genlocked).

In addition to the above video sources, the following video sources are supported when running in single-Full configuration:

	Video sources supported
Camera Link Standard	• Eight tap x 8-bit. • Ten tap x 8-bit. (sequential taps)
Not Camera Link Standard	• Four tap x 14-16-bit.

❖ Note that Matrox Solios eV-CL boards can simultaneously write to a limited number of non-sequential memory regions; this further restricts the tap configurations supported. For the supported number of non-sequential memory regions, see the *Acquisition controller* section, later in this chapter.

Matrox Solios eV-CLB and eV-CLBL support power over Camera Link (PoCL) and non-PoCL compliant video sources. For compatibility with non-PoCL video sources, Matrox Solios eV-CLB and eV-CLBL feature SafePower mode to supply power only after determining whether the connected video source is PoCL compliant. The PoCL protection on-board fuse can sustain a current of 0.4 A.

ChannelLink receivers

Matrox Solios eV-CLB and eV-CLBL have two ChannelLink receivers that can be used asynchronously in dual-Base configuration or synchronously in single-Medium configuration. Matrox Solios eV-CLF and eV-CLFL have three ChannelLink receivers that can only be operated synchronously; in single-Medium configuration, they only use two of the receivers, whereas in single-Full configuration, they use all three receivers.

For Matrox Solios eV-CLB and eV-CLBL, each ChannelLink receiver can receive up to 24 bits of video data and 4 bits of synchronization and field data from the video source, as serialized data over four LVDS pairs; a clock is received from the video source over a fifth LVDS pair.

For Matrox Solios eV-CLF and eV-CLFL, the first ChannelLink receiver has the capabilities of the ChannelLink receivers on Matrox Solios eV-CLB and eV-CLBL. In single-Medium configuration, the second ChannelLink receiver can only receive up to 24 bits of video data and the third ChannelLink receiver is not used. In single-Full configuration, the second and third ChannelLink receivers can each receive 28 bits of video data.

The ChannelLink receivers can operate at frequencies of 20 MHz to 85 MHz.

Demultiplexers to support time-multiplexed video sources

Each acquisition path of the board features a demultiplexer. It can deserialize input from time-multiplexed video sources on a clock cycle basis. Time-multiplexed video sources can output larger pixel depths and more taps than are possible with non-time-multiplexed video sources in the same configuration (with the same amount of cabling). When enabled, the demultiplexer assumes that two video streams share the same data path and that the streams are interleaved based on the clock cycle. The demultiplexer assumes that on one clock cycle, the data is from one stream and that on the next clock cycle, the data is from another stream. The demultiplexer can only deserialize video inputs that, when combined and, if necessary, expanded, total a maximum depth of 64 bits per acquisition path.

Expansion refers to the automatic addition of padding zeros on the most significant bits (MSB) of 10-, 12-, and 14-bit data to create byte aligned 16-bit data. Expansion is not always necessary.

Lookup tables

Matrox Solios eV-CL has on-board lookup tables (LUTs) that can be used to precondition input data at acquisition time, before it is stored in an image buffer.

The LUTs on Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration can be operated in the following configurations per acquisition path[1]:

- 8 palettes of one, two, three, or four 256-entry 8-bit LUTs.
- 4 palettes of one or two 1024-entry 8- or 16-bit LUTs.
- 1 palette of one or two 4096-entry 8- or 16-bit LUTs.

1. For example, two 1024-entry 8-bit LUTs can map 2-tap 10-bit data to 8-bit values. In addition, one 1024-entry 8-bit LUT can map 1-tap 10-bit data to 8-bit values.

The LUTs on Matrox Solios eV-CLB and eV-CLBL in single-Medium configuration and those on Matrox Solios eV-CLF and eV-CLFL can be operated in the following configurations:

- 8 palettes of one, two, three, four, or eight 256-entry 8-bit LUTs.
- 4 palettes of one, two, three, or four 1024-entry 8- or 16-bit LUTs.
- 1 palette of one, two, three, or four 4096-entry 8- or 16-bit LUTs.

Instead of being mapped through a LUT, 14- and 16-bit data by-pass the LUTs.

The LUTs are programmed using the MIL-Lite function **MdigLut**().

Communication

For each acquisition path, two LVDS pairs are used to transmit and receive asynchronous serial communication between the video source and the board. These signals are handled by the Universal Asynchronous Receiver/Transmitters (UARTs).

For each acquisition path, four camera control output signals are also available. These are general-purpose signals that are sent to the video source.

UARTs

Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration offer two LVDS-compatible Matrox serial interfaces. Matrox Solios eV-CLB and eV-CLBL, in single-Medium configuration, and Matrox Solios eV-CLF and eV-CLFL offer a single LVDS-compatible Matrox serial interface. Each interface is mapped as a COM/ttyS port so that it can be accessed through the operating system communication API. Each interface is comprised of both a transmit port and a receive port, permitting the interface to work in full-duplex mode. The interfaces are located on the Camera Link connectors.

Each interface is controlled by a universal asynchronous receiver-transmitter (UART)[1]. Each UART features independently programmable baud rates, supporting all standard baud rates from 300 baud up to 230400[2] baud.

PSGs

Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration feature two programmable synchronization generators (PSGs). Matrox Solios eV-CLB and eV-CLBL, in single-Medium configuration, and Matrox Solios eV-CLF and eV-CLFL feature one PSG. Each PSG allows for independent acquisition from one video source, since they are responsible for managing all video timing and synchronization signals.

The PSGs are also responsible for managing the camera control and auxiliary signals supported by the board. These signals are configurable signals that can support one or several functions, one of which is user-defined; the table in the next subsection identifies the functions to which the camera control and auxiliary signals can be defined. The PSGs are also responsible for implementing the functionality to which these can be defined.

Camera control and auxiliary signals

The following table summarizes the auxiliary functionality that the PSGs support, and the corresponding signals that the PSGs can receive/generate on Matrox Solios eV-CLB and Matrox Solios eV-CLF. For example, P0_TTL_AUX_IO_0 can be defined as an exposure output (from M_TIMER3), trigger input (M_HARDWARE_PORT8), field polarity input, or user-defined input/output (M_USER_BIT... + 2) signal.

1. The UART implementation was derived from a design by Daniel Wallner. Please see *Appendix C: Acknowledgments* for copyright information.
2. The maximum baud rate is highly dependent on the amount of computer resources available.

Type of signal (MIL constant where *n* = # in table)	Acquisition path	LVDS cam. ctrl								TTL aux I/O						OPTO aux in				LVDS aux in				LVDS aux out	
		Camera Link Connector								Aux I/O Connector						Aux I/O Connector				Aux I/O Connector				Aux I/O Connector	
		0				1				0			1			0		1		0		1		0	1
		CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	P0_TTL_AUX_IO_0	P0_TTL_AUX_IO_1	TTL_AUX_IO_0	P1_TTL_AUX_IO_0	P1_TTL_AUX_IO_1*	TTL_AUX_IO_1*	P0_OPTO_AUX_IN0	P0_OPTO_AUX_IN1	OPTO_AUX_IN0	OPTO_AUX_IN1	P0_LVDS_AUX_IN0	P0_LVDS_AUX_IN1	LVDS_AUX_IN0	LVDS_AUX_IN1*	P0_LVDS_AUX_OUT0	P1_LVDS_AUX_OUT0*
Exposure output (M_TIMER*n*)	0	1/2	1/2	1/2	1/2					3	1/4	2												1	
	1					1/2	1/2	1/2	1/2				3	1/4	2										1
Trigger input† (M_HARDWARE_PORT*n* and trigger controller affected)	0									8 (T0)	9 (T1)	2 (T2)			3 (T3)	6 (T0)	7 (T1)	0 (T2)	1 (T3)	10 (T0)	11 (T1)	4 (T2)	5 (T3)		
	1											2 (T2)	8 (T0)	9 (T1)	3 (T3)			0 (T0/ T2)	1 (T1/ T3)			4 (T0/ T2)	5 (T1/ T3)		
Field polarity input	0									0						0				0					
	1												0					0				0			
Timer-clock input	0																				0				
	1																						0		
Quadrature input‡	0																			0	1				
	1																					0	1		
User-defined input (M_USER_BIT... + *n*)	0									2	3	4			5	12	13	8	9	10	11	6	7		
	1											4	2	3	5			8	9			6	7		
User-defined output (M_USER_BIT... + *n*)	0	M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1					2	3	4			5									0	
	1					M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1			4	2	3	5										0

. Not available when the DB-15 auxiliary I/O connector is replaced with the optional DB-9 connector from the SOLEVAACC01PAK accessory kit.

†. Note that there are only 4 trigger controllers per acquisition path. T# indicates the trigger controller to which an auxiliary signal can be routed; the other number indicates the MIL M_HARDWARE_PORT number to use to define that auxiliary signal as a trigger input signal. For example, P0_OPTO_AUX_IN0, P0_TTL_AUX_IO_0, or P0_LVDS_AUX_IN0 can be used as a trigger input signal to trigger controller 0 for acquisition path 0 (M_DEV0); to define one of these signals as such, use M_HARDWARE_PORT6, M_HARDWARE_PORT8, or M_HARDWARE_PORT10, respectively.

‡. Note that a rotary encoder with quadrature output transmits a two-bit code. The table entries 0 and 1, therefore, denote bit position.

The following tables summarize the auxiliary functionality that the PSGs support, and the corresponding signals that the PSGs can receive/generate on Matrox Solios eV-CLBL and Matrox Solios eV-CLFL. For example, P0_TTL_AUX_IO_0 can be defined as an exposure output (from M_TIMER3), trigger input (M_HARDWARE_PORT8), field polarity input, or user-defined input/output (M_USER_BIT... + 2) signal.

Type of signal (MIL constant where *n* = # in table)	Path#	Max # signals*	LVDS cam. ctrl								TTL aux. I/O†						OPTO aux. in†				LVDS aux. in†				LVDS aux. out†			
			Camera Link connector 0				Camera Link connector 1																					
			CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	P0_TTL_AUX_IO_0‡	P0_TTL_AUX_IO_1	P1_TTL_AUX_IO_0	P1_TTL_AUX_IO_1	TTL_AUX_IO_0	TTL_AUX_IO_1	P0_OPTO_AUX_IN0‡	P0_OPTO_AUX_IN1‡	OPTO_AUX_IN0	OPTO_AUX_IN1	P0_LVDS_AUX_IN0‡	P0_LVDS_AUX_IN1	LVDS_AUX_IN0	LVDS_AUX_IN1	P0_LVDS_AUX_OUT0	P0_LVDS_AUX_OUT1	P1_LVDS_AUX_OUT0	P1_LVDS_AUX_OUT1
Exposure output (M_TIMER*n*)	0	4	1/2	1/2	1/2	1/2					3	1/4			2										1	2		
	1	4					1/2	1/2	1/2	1/2			3	1/4		2											1	2
Trigger input ** **(M_HARDWARE_PORT*n* and trigger controller affected)**	0	4									8 (T0)	9 (T1)			2 (T2)	3 (T3)	6 (T0)	7 (T1)	0 (T2)	1 (T3)	10 (T0)	11 (T1)	4 (T2)	5 (T3)				
	1	4											8 (T0)	9 (T1)	2 (T2)	3 (T3)			0 (T0/ T2)	1 (T1/ T3)			4 (T0/ T2)	5 (T1/ T3)				
Field polarity input	0	1									0						0				0							
	1	1											0						0				0					
Timer-clock input	0	1																				0						
	1	1																						0				
Quadrature input††	0	1																			0	1						
	1	1																					0	1				
User-defined input (M_USER_BIT... + *n*)	0	12									2	3			4	5	12	13	8	9	10	11	6	7				
	1	8											2	3	4	5			8	9			6	7				
User-defined output (M_USER_BIT... + *n*)	0	7	M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1					2	3			4	5									0	1		
	1	7					M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1	M_ CC0/ CC1			2	3	4	5											0	1

*. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.

†. On external auxiliary I/O connector 0 (DB-44).

‡. On external auxiliary I/O connector 1 (DB-9).

**. Note that there are only 4 trigger controllers per acquisition path. T# indicates the trigger controller to which an auxiliary signal can be routed; the other number indicates the MIL M_HARDWARE_PORT number to use to define that auxiliary signal as a trigger input signal. For example, P0_OPTO_AUX_IN0, P0_TTL_AUX_IO_0, or P0_LVDS_AUX_IN0 can be used as a trigger input signal to trigger controller 0 for acquisition path 0 (M_DEV0); to define one of these signals as such, use M_HARDWARE_PORT6, M_HARDWARE_PORT8, or M_HARDWARE_PORT10, respectively.

††. Note that a rotary encoder (starting with Matrox Solios XCL Version 100) with quadrature output transmits a two-bit code. The table entries denote bit position.

Type of signal	Path#	Max # signals*	LVDS cam. ctrl								Received with data		LVDS dedicated signals† ‡
			CL connect. 0				CL connect. 1				CL connect. 0	CL connect. 1	
			CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4			
Frame valid input	0	1									0		
	1	1										0	
VSYNC output	0	1	0	0	0	0							**P0_LVDS_VSYNC_OUT**
	1	1					0	0	0	0			**P1_LVDS_VSYNC_OUT**
Line valid input	0	1									0		
	1	1										0	
HSYNC output	0	1	0	0	0	0							**P0_LVDS_HSYNC_OUT**
	1	1					0	0	0	0			**P1_LVDS_HSYNC_OUT**
Data valid input	0	1									0		
	1	1										0	
Clock input	0	1											**Xclk (CL connect. 0)**
	1	1											**Xclk (CL connect. 1)**
Clock output	0	1	0	0	0	0							**P0_LVDS_CLK_OUT**
	1	1					0	0	0	0			**P1_LVDS_CLK_OUT**

*. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.

†. In this column, each signal is a dedicated signal (that is, it cannot be redefined as another type of signal).

‡. Clock input is received on the Camera Link connectors, whereas the other signals in this column are received on/transmitted from external auxiliary I/O connector 0 (DB-44).

Specifications of the auxiliary signals and camera control signals

Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration have auxiliary/camera control signals in the following formats:

Auxiliary signals	# per path	# total*
LVDS camera control output signals	4	8
TTL auxiliary input or output signals	2 (+2 not for a specified path)	6
Opto-isolated auxiliary input signals	2 reserved for P0, 2 not for a specified path	4
LVDS auxiliary input signals	2 reserved for P0, 2 not for a specified path	4
LVDS auxiliary output signals†	1 or 2	2 or 4

. This is the number of auxiliary signals available when using the DB-15 auxiliary I/O connector on the cable adapter bracket; if using the optional cable adapter bracket with the DB-9 connector from the SOLEVAACC01PAK accessory kit, less auxiliary signals are available (see the pinout of the auxiliary I/O connector in *Appendix B: Technical information*).

†. The Matrox Solios eV-CLBL has 2 LVDS auxiliary output signals per path, for a total of 4 signals in dual-Base configuration.

Matrox Solios eV-CLB and eV-CLBL, in single-Medium configuration, and Matrox Solios eV-CLF and eV-CLFL have auxiliary/camera control signals in the following formats:

Auxiliary signals	# total
LVDS camera control output signals	4
TTL auxiliary input or output signals	4
Opto-isolated auxiliary input signals	4
LVDS auxiliary input signals	4
LVDS auxiliary output signals	2

When an auxiliary input signal is received in TTL format directly, it will be clamped at a maximum of 5.7 V and at a minimum of -0.7 V to protect the input buffer. Typically, the signal should have a maximum of 5 V and a minimum of 0 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low.

The opto-isolated auxiliary input signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and allows the frame grabber to be totally isolated. The voltage difference across the positive and negative components of the signal must be between 4.06 V and 9.165 V for logic high, and between -5.0 V and 0.8V for logic low.

You specify the purpose of the camera control and auxiliary signals in the DCF. You can then program these signals using the MIL-Lite function **MdigControl**() with M_USER..., M_TRIGGER..., M_GRAB_EXPOSURE..., or M_ROTARY_ENCODER...

Exposure timers

Each PSG has four exposure timers. These timers can each generate an exposure output signal with up to two pulses; exposure output signals allow you to control the exposure time and other external events related to the video source (such as a strobe). The exposure signals can be output using camera control signals or auxiliary output signals (or auxiliary I/O signals in output mode).

Each PSG has two 24-bit timers (Timer 0 and 1) and two 16-bit timers (Timer 2 and 3). The 24-bit timers can count up to 16777215 clock ticks before resetting; the 16-bit timers can count up to 65535 clock ticks before resetting.

The exposure timers can use one of the following as a clock source:

- **A clock that is internally generated.** Each exposure timer can use its PSG's clock generator, which can generate a single clock with a programmable frequency of 0.8 to 100 MHz. Timers can only use the clock generator of their own PSG.

- **A clock from an external source.** In this case, you must define the appropriate auxiliary input signal as a timer-clock input; the timer-clock input signal must meet the specification of the auxiliary signal. The same timer-clock input can be used to clock different timers of the same PSG.

- **A clock based on another exposure timer of the same PSG.** Timer 0 can use a clock based on Timer 1, and Timer 1, 2, and 3 can use a clock based on Timer 0.

- **A clock based on an external pixel clock signal.** This applies to Matrox Solios eV-CLBL and Matrox Solios eV-CLFL only.

- **A clock based on the HSYNC or VSYNC signal generated by the PSG.** This applies to Matrox Solios eV-CLBL and Matrox Solios eV-CLFL only.

To output an exposure signal, use the MIL-Lite function **MdigControl**() with **M_GRAB_EXPOSURE**. Set the clock source of an exposure timer in the DCF.

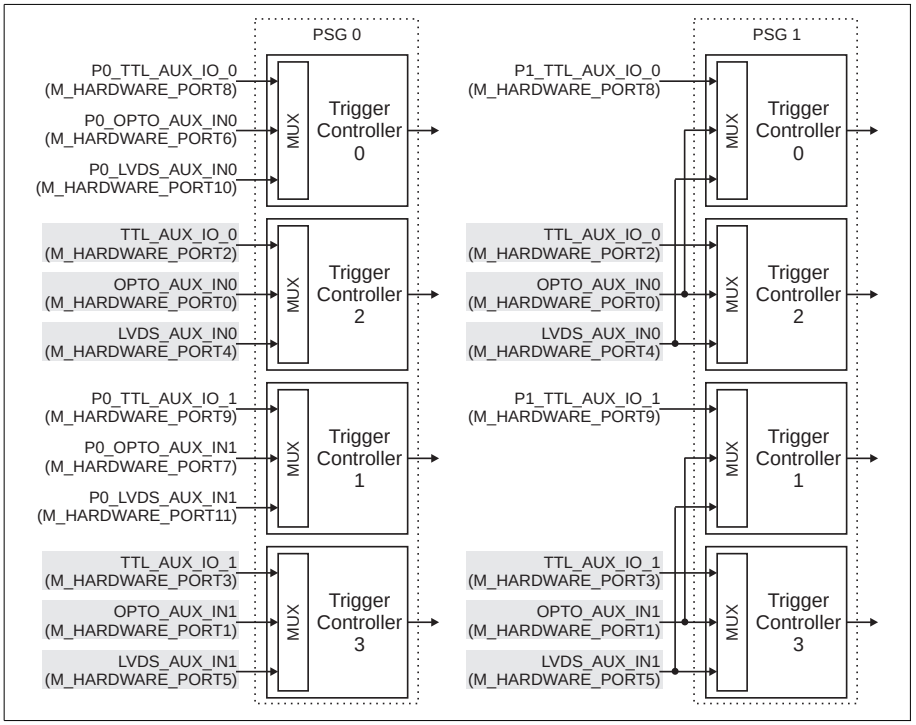
Next valid frame/field and asynchronous reset modes

Matrox Solios eV-CL can operate in two modes: next valid frame/field mode or asynchronous reset mode. In next valid frame/field mode, the board waits for the next valid frame or field (as specified by the DCF file) before commencing the grab.

In asynchronous reset mode, the board resets the video source to begin a new frame when a trigger signal is received. The board uses an exposure timer signal to reset the video source.

Trigger

Whether in next valid frame/field mode or in asynchronous reset mode, the board accepts trigger input signals, which allow image acquisition to be synchronized with external events. Each PSG has 4 trigger controllers. Multiple auxiliary signals can trigger a trigger controller; however, you can program only one per trigger controller as a trigger input signal.



The trigger input signal must meet the specification of the auxiliary signal.

If using the trigger to start acquisition, the trigger signal's pulse width must be greater than two pixels; if using the trigger to start the exposure timer, the trigger signal's pulse width must be greater than two clock periods of the timer. To determine the timer period, take the inverse of the pixel or timer's clock frequency, respectively. For example, if the pixel frequency is 12.27 MHz, the minimum pulse width is 2 x 1/12.27 MHz (approximately 163 nsec).

To grab upon a trigger, use the MIL-Lite function **MdigControl**() with **M_GRAB_TRIGGER**. To start an exposure timer upon a trigger, use **MdigControl**() with **M_GRAB_EXPOSURE_SOURCE**.

Synchronization

For each PSG in Matrox Solios eV-CLBL and Matrox Solios eV-CLFL the board can supply one horizontal (HSYNC) and one vertical (VSYNC) synchronization signal to the video source. Through the Camera Link connectors, the board also receives synchronization data (frame valid, line valid, and data valid) along with the video data; refer to the Camera Link specification for a description of the synchronization data.

Note that the Camera Link standard does not regulate how to transmit an interlaced video signal; however, you can define an auxiliary signal as a field polarity input signal and transmit the field polarity on this signal.

Clock

For each PSG in Matrox Solios eV-CLBL and Matrox Solios eV-CLFL, the board can supply a clock signal to the video sources. Through each of the video input Camera Link connectors, the board can also receive a clock signal.

Quadrature decoder

The PSGs of the Matrox Solios eV-CL board feature a quadrature decoder that can decode input from a rotary encoder with quadrature output. This type of encoder (a quadrature encoder) is a device that provides information about the absolute position and direction of a rotating shaft. The encoder outputs a two-bit code (also known as gray code) on two pairs of LVDS wires in a precise sequence, as shown in the table below.

Channel	Quadrant A	Quadrant B	Quadrant C	Quadrant D
Quadrature channel A	0	1	1	0
Quadrature channel B	0	0	1	1

From this sequence, the position of the rotating shaft and the direction of rotation can be determined.

The quadrature decoder can decode gray code and update a 32-bit internal counter. The sequence going from Quadrant A through Quadrant B through Quadrant C through Quadrant D decrements the 32-bit internal counter. You can read the counter at different stages of the grab or trigger a grab based on the value of the counter. The quadrature decoder supports a maximum encoder frequency equal to 1/3 of the pixel clock frequency of the video source.

The LVDS receivers of the Matrox Solios eV-CL board support 5 V tolerant rotary encoders.

❖ Note that an external source must be used to power the rotary encoder (for example, the computer's 5 V power source).

For each PSG, you can program two auxiliary signals as quadrature input signals. One to carry the first bit, and one to carry the second. You can toggle quadrature decoder settings using the MIL-Lite function **MdigControl**(), or by modifying the DCF file.

User-defined signals

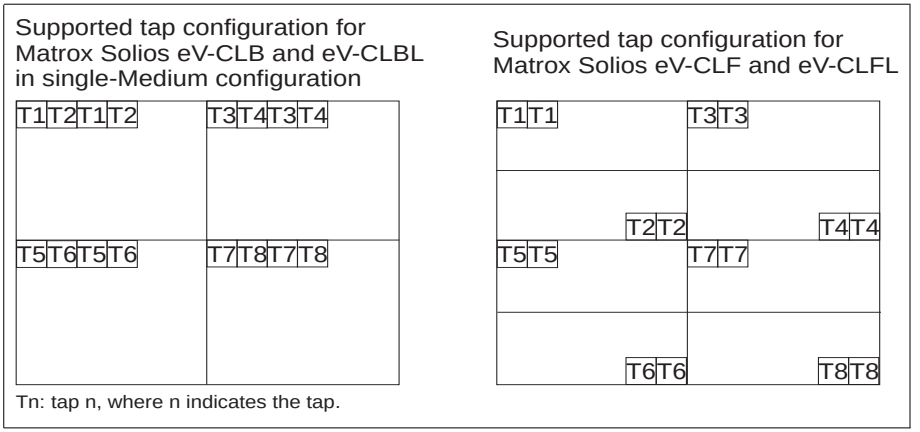
Any auxiliary signal can be configured as a user-defined signal. You can route any input signal that meets specifications to an auxiliary input signal (or auxiliary I/O signals in input mode) configured as a user-defined signal; your application can then interpret this user-defined signal as required.

You can specify the on/off state of a required output signal and have the PSG generate and route it to an auxiliary output signal (or auxiliary I/O signals in output mode) configured as a user-defined signal; your application can set the on/off state of the signal based on some analysis.

To inquire and control user-defined signals, use the MIL-Lite functions **MdigInquire**() and **MdigControl**() with **M_USER_BIT_...**

Acquisition controller

The acquisition controller is responsible for reconstructing and storing image data in on-board acquisition memory. On Matrox Solios eV-CLB and eV-CLBL, the acquisition controller can write to two non-sequential memory regions per acquisition path in dual-Base configuration; whereas the acquisition controller can write to four non-sequential memory regions per acquisition path in single-Medium configuration. On Matrox Solios eV-CLF and eV-CLFL, the acquisition controller can write to eight non-sequential memory regions per acquisition path, regardless of the configuration.



To establish the number of non-sequential memory regions to which your video source must write, refer to the documentation accompanying your video source.

When writing data to memory, the acquisition controller can perform line and frame reversal; it can flip the image horizontally and/or vertically.

Video formatter

The video formatter is capable of high-speed transfers from acquisition memory, through the PCI-X to PCIe bridge, to Host memory, off-board display memory, or other devices across the Host bus. Upon transmitting the video data, the video formatter can also format the data as follows:

- **Resizing.** Image data can be cropped (ROI capture) and/or subsampled. This can be useful to implement custom software-based motion detection because at a reduced scale, image comparison is faster. The video formatter can subsample in the horizontal direction by integer factors of 1 to 16; whereas, there is no restriction in the vertical direction; subsampling occurs using nearest-neighbor interpolation.

- **Flipping.** Image data can be flipped vertically.

- **Bayer color decoding (only on Matrox Solios eV-CLB and eV-CLBL).** Supports decoding the color information of a single-band, Bayer color-encoded image; the video formatter supports GBRG, GRBG, BGGR, and RGGB patterns. While decoding, the video formatter can also perform white balance correction. It uses a 2x2 neighborhood demosaicing algorithm.

- **Color space conversion.** Converts grabbed image data to various color formats and bit-depths. The color space converter can also perform color kill, which converts the data to grayscale and then converts it to the appropriate destination format.

Image data can be converted as follows:

In	Out							
	8-bit monochrome	16-bit monochrome	24-bit packed BGR	32-bit packed BGRa	48-bit packed BGR	16-bit YUV (YUYV)	24-bit RGB planar	48-bit RGB planar
8-bit monochrome	yes		yes	yes		yes	yes	
16-bit monochrome	yes	yes	yes	yes		yes	yes	
24-bit packed BGR	yes		yes	yes		yes	yes	
48-bit packed BGR	yes		yes	yes	yes	yes	yes	yes

The equations for the YUV16 conversion are described in the following table:

Color space conversion	Equations
RGB-to-YUV	• Y = 0.299 R + 0.587 G + 0.114 B • U = -0.169 R - 0.331 G +0.500 B + 128 • V = 0.500 R - 0.419 G - 0.081 B +128
BGR-to-YUV	• Y = 0.114B + 0.587G +0.0229R • U = 0.500B - 0.331G - 0.169R + $2^{(res-1)}$ • V = -0.081B - 0.419G + 0.500R + $2^{(res-1)}$

Formatting/ converting data when grabbing into Host buffers

When you grab into a Host buffer (for example, using the MIL-Lite function **MdigGrab**()), use **MdigControl**() with M_SOURCE_OFFSET_X/Y, M_SOURCE_SIZE_X/Y, and/or M_GRAB_SCALE_X/Y to crop or resize image data when grabbing.

The video formatter is not used to flip images grabbed into Host buffers; the acquisition controller is responsible for this task. For more information, see the *Acquisition controller* section, earlier in this chapter. To flip image data when grabbing, use **MdigControl**() with M_GRAB_DIRECTION_X/Y.

While grabbing, the video formatter automatically converts the bit-depth and color format of the source image to the bit-depth and color format of the destination buffer. The DCF establishes the source image data, while the destination grab buffer, allocated using **MbufAlloc...**(), establishes the output image data. If your camera and DCF are in Bayer mode, the Matrox Solios eV-CLB and eV-CLBL will decode the Bayer color-encoded image before it applies color space conversion.

Memory

Matrox Solios eV-CL has on-board acquisition memory. It has 128, 256, or 512 Mbytes of linearly addressable 32-bit 216 MHz DDR2 SDRAM to store acquisition data. This memory has a memory bandwidth of 1.73 Gbytes/sec.

PCI-X to PCIe bridge

The PCI-X to PCIe bridge handles the Matrox Solios eV-CL board's PCIe connection to the Host. On-board, Matrox Solios eV-CL uses PCI-X technology to communicate. To communicate with the Host, Matrox Solios eV-CL transfers data using the Host's PCIe bus. The PCI-X to PCIe bridge handles the protocol conversion.

Using the Host PCIe bus, Matrox Solios eV-CL can copy data between its acquisition memory, the Host, and any other memory mapped onto the PCIe bus (for example, display memory).

Important

Note that transfer of image data to a display board might require intervention from the Host CPU, depending on your computer's architecture.

Under optimum conditions, Matrox Solios eV-CL can exchange data with the Host at a peak transfer rate of up to 1 Gbyte/sec; the maximum achievable bandwidth depends on the type of camera and digitizer configuration format (DCF) used. Optimum conditions include using the board in a PCIe slot with 4 active lanes.

Using the PCIe bus, Matrox Solios eV-CL can also access Host physically contiguous, non-paged memory. An advantage of this memory is that a bus mastering device (such as Matrox Solios eV-CL) can access this memory without the help of the Host CPU.

Appendix A: Glossary

This appendix defines some of the specialized terms used in the Matrox Solios eV-CL documentation.

Glossary

- **Bandwidth**

  A term describing the capacity to transfer data. Greater bandwidth is needed to sustain a higher transfer rate. Greater bandwidth can be achieved, for example, by using a wider bus.

- **Blanking period**

  The portion of a video signal after the end of a line or frame, and before the beginning of a new line or frame. During this period, the video signal is "blank" so that a scan line can be brought back to the beginning of the new line or frame. The portion of a video signal after the end of a line and before the beginning of a new line is known as the *horizontal blanking period*. The portion of a video signal after the end of a frame and before the beginning of a new frame is known as the *vertical blanking period*.

- **Contiguous memory**

  A block of memory occupying a single, unbroken series of addresses.

- **DCF**

  Digitizer Configuration Format. A file format that defines the input data format and, for example, how to accept or generate video timing signals, such as horizontal sync, vertical sync, and pixel clock.

  Such files have a *.dcf* extension.

- **DDR2 SDRAM**

  Double Data Rate2 Synchronous Dynamic Random Access Memory. A type of memory used for image capture and processing. SDRAM allows the Matrox Solios eV-CL to access data at very high speed, which is important for I/O-bound functions.

- **Digitizer Configuration Format**

  See DCF.

- **Double buffering**

  Alternating the destination of an operation between two buffers. Double buffering allows you to, for example, process one buffer while grabbing into the other buffer.

- **Dynamic range**

  The range of values present in a buffer. An unsigned 8-bit buffer, for example, has an allowable range of 0 to 255; its dynamic range can be any range within these values.

- **Exposure signal**

  The signal generated by one of the programmable timers of the frame grabber module. The exposure signal can be used to control external hardware. For example, it can be fed to the video source to control its exposure time or used to fire a strobe light.

- **Exposure time**

  Refers to the period during which the image sensor of a video source is exposed to light. As the length of this period increases, so does the image brightness.

- **Field**

  One of the two halves that together make up the image grabbed from an interlaced video source. One half consists of the image's odd lines (known as the *odd field*); the other half consists of the image's even lines (known as the *even field*).

- **FPGA**

  Field-programmable gate array. An array of digital electronic components that can be programmed to perform a specific function. An FPGA can contain logic gates, lookup tables, flip-flops and programmable interconnect wiring. This combination of customizability and functionality allows for the same FPGA design to be used in a variety of projects.

- **Frame**

  A single image grabbed from a video source.

- **Gain level**

  The factor by which an analog input signal is scaled. The gain affects the brightness and contrast of the resulting image.

- **Grab**

  To acquire an image from a video source.

- **Horizontal blanking period**

  The portion of a video signal after the end of a line and before the beginning of a new line. During this period, the video signal is "blank".

  See also *vertical blanking period*.

- **Horizontal synchronization signal**

  The part of a video signal that indicates the end of a line and the start of a new one.

  See also *vertical synchronization signal*.

- **Interlaced scanning**

  Describes a transfer of data in which the odd-numbered lines of the source are written to the destination buffer first, and then the even-numbered lines (or vice-versa).

  See also *progressive scanning*.

- **Latency**

  The time from when an operation is started to when the final result is produced.

- **LUT mapping**

  Lookup table mapping. A point-to-point operation that uses a table to define a replacement value for each possible pixel value in an image.

- **LVDS**

  Low-voltage differential signalling. LVDS offers a general-purpose, high bandwidth interface standard for serial and parallel data interfaces that require increased bandwidth at high speed, with low noise and power consumption.

- **Progressive scanning**

  Describes a transfer of data in which the lines of the source are written sequentially into the destination buffer.

  See also *interlaced scanning*.

- **Real-time processing**

  The processing of an image as quickly as the next image is grabbed.

  Also known as *live processing*.

- **Rotary encoder**

  A device used to convert the angular position of a shaft or axle to an analog or digital code.

- **Saturate**

  To replace overflows (or underflows) in an operation with the highest (or lowest) possible value that can be held in the destination buffer of the operation.

- **UART**

  Universal Asynchronous Receiver/Transmitter. A component that handles asynchronous communication through a serial interface (for example, RS-232 or LVDS).

- **Vertical blanking period**

  The portion of a video signal after the end of a frame and before the beginning of a new frame. During this period, the video signal is "blank".

  See also *horizontal blanking period*.

- **Vertical synchronization signal**

  The part of a video signal that indicates the end of a frame and the start of a new one.

  See also *horizontal synchronization signal*.

Appendix B: Technical information

This appendix contains information that might be useful when installing your Matrox Solios eV-CL board.

Board summary

Global information

- Operating system: See your software manual for supported versions of Microsoft Windows and Linux.

- Minimum computer requirements:

  - x4 (or better) PCIe slot.

  - Processor with an Intel 32-bit architecture (IA32) or equivalent.

  - A relatively up-to-date PCIe chipset. The list of platforms that are known to be compatible with Matrox Solios eV-CL are available on the Matrox website, under the board's PC compatibility list.

  - A proper power supply. Refer to the *Electrical specifications* section.

  Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Technical features of Matrox Solios eV-CL

Features common to all Matrox Solios eV-CL boards

- Has a x4 PCIe Host interface.

- Supports a maximum clock frequency of up to 85 MHz. Clock frequency is also dependent on the length of the cable used. The following are rough guidelines for the maximum clock frequencies that can be achieved; contact your cable manufacturer for the actual maximum clock frequency that can be achieved for your specific cable.

Maximum cable length (m)	Maximum clock frequency (MHz)*
10	70
7	80
5	85

*. Achieved with high quality cables.

- Supports frame and line-scan video sources. The min/max length for an image and min/max width for a line are as follows:

Resolution	Minimum pixels per line	Maximum pixels per line
8-bit monochrome	17	65535
16-bit monochrome	17	32767
24-bit color	17	21845
48-bit color	17	10922

- Can convert captured data to RGB24, RGB32, or YUV16 format. In addition, data can be converted to 8-bit, 10-bit, 12-bit, 14-bit and 16-bit monochrome data.

- Supports line reversal and frame reversal during acquisition. Can only perform frame reversal during data transfer to Host.

- Can crop (ROI capture) acquired data or subsample it by integer subsampling factors of 1 to 16.
- Has 128/256/512 Mbytes of 32-bit 216 MHz DDR2 SDRAM used as acquisition memory. 1728 Mbytes/sec of memory bandwidth.
- Has one LVDS serial port (UART) per acquisition path.
- Supports an external 5 V tolerant rotary encoder with quadrature output per acquisition path.
- Has four camera control signals (exposure or user-defined output) per acquisition path[1].
- Three TTL auxiliary I/O signals (trigger, field polarity, or user-defined input, or exposure or user-defined output) per acquisition path[1].
- Two LVDS auxiliary input signals (trigger, field polarity, timer-clock, quadrature, or user-defined input) per acquisition path[1].
- Two opto-isolated auxiliary input signals (trigger, field polarity, or user-defined input) per acquisition path[1].

1. See the *Matrox Solios eV-CL hardware reference* chapter for supported configurations.

Features specific to Matrox Solios eV-CLB and eV-CLBL in dual-Base configuration

- Has two independent acquisition paths. Each supports a video source in the Camera Link Base configuration.
- Can provide power over Camera Link (PoCL) with SafePower. The PoCL protection on-board fuse can sustain a current of 0.4 A.
- Supports decoding the color information of a single-band, Bayer color-encoded image. While decoding, the boards can also perform white balance correction.
- Has programmable LUTs that can be operated in the following configurations per acquisition path[1]:
  - 8 palettes of one, two, three, or four 256-entry 8-bit LUTs.
  - 4 palettes of one or two 1024-entry 8- or 16-bit LUTs.
  - 1 palette of one or two 4096-entry 8- or 16-bit LUTs.
- Instead of being mapped through a LUT, 14- and 16-bit data by-pass the LUTs.

Features specific to Matrox Solios eV-CLB and eV-CLBL in single-Medium configuration and to Matrox Solios eV-CLF and eV-CLFL

- Has a single acquisition path. The board supports a single video source in the Camera Link Medium or Full configuration.
- The programmable LUTs can be operated in the following configurations:
  - 8 palettes of one, two, three, four, or eight 256-entry 8-bit LUTs.
  - 4 palettes of one, two, three, or four 1024-entry 8- or 16-bit LUTs.
  - 1 palette of one, two, three, or four 4096 entry 8- or 16-bit LUTs.
- Instead of being mapped through a LUT, 14- and 16-bit data by-pass the LUTs.

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1. For example, two 1024-entry 8-bit LUTs can map 2-tap 10-bit data to 8-bit values. In addition, one 1024-entry 8-bit LUT can map 1-tap 10-bit data to 8-bit values.

Features specific to Matrox Solios eV-CLB and Matrox Solios eV-CLF

- One additional LVDS auxiliary output signal (exposure or user-defined output) per acquisition path[1].

Features specific to Matrox Solios eV-CLBL and Matrox Solios eV-CLFL

- Separate LVDS pixel clock, HSYNC, and VSYNC output signals per acquisition path.

- Two additional LVDS auxiliary output signal (exposure or user-defined output) per acquisition path[1].

1. See the *Matrox Solios eV-CL hardware reference* chapter for supported configurations.

Electrical specifications

Matrox Solios eV-CL (starting from version 000)	
Operating voltage and current (eV-CL)	Typical 3.3 V: 1 A, 3.3 W Max. PoCL 12.0 V: 800 *mA*, 9.6 W* (Current directly drawn from the slot. Power is not dissipated by the board; it is only used by the camera). Total dissipated by board and PoCL cameras = 3.3 W + 9.6 W = 12.9 W
I/O Specifications	
Input signals in LVDS format	100 Ohm differential termination. Input current: -10 µA (min) to +10 µA (max). Input voltage: common-mode: 0.1 V (min) to 2.3 V (max). differential threshold: low of -100 mV (min); high of 100 mV (max).
Output signals in LVDS format	No termination. Output current (loaded 100 Ohm): 20 mA (typ). Output voltage (loaded 100 Ohm): differential: 250 mV (min) to 450 mV (max). common-mode: 1.125 V (min) to 1.375 V (max). low: 1.02 V (typ), 0.9 V (min); high: 1.33 V (typ), 1.6 V (max).
Input signals in TTL format	No termination. Pulled up to 3.3 V with 4.716 kOhm. Clamped to -0.7 V and to 5.7 V. Input current: 1 µA (max). Input voltage threshold: low of 0.8 V (max); high of 2.0 V (min).
Output signals in TTL format	27 Ohm series termination. High-level output current: -32 mA (max). Low-level output current: +64 mA (max). Output voltage: low of 0.55 V (max); high of 3.0 V (min) at -3 mA, 2.0 V (min) at -32 mA.
Opto-coupled input signals†	511 Ohm series termination (connected on the anode inputs of the opto-coupler device). Input current: low: 250 µA (max). high: 5 mA (min) (6.3 mA recommended) to 15 mA (max) (10 mA recommended). Input voltage (with 511 Ohm series resistor only): low of 0.8 V (max); high of 4.06 V (min) (4.72 V recommended).

*. The PoCL protection on-board fuse on Matrox Radient eCL can sustain a current of 0.4 A.

†. The Matrox Solios eV-CL opto-couplers are manufactured by Agilent Technologies (P/N HCPL-0631).

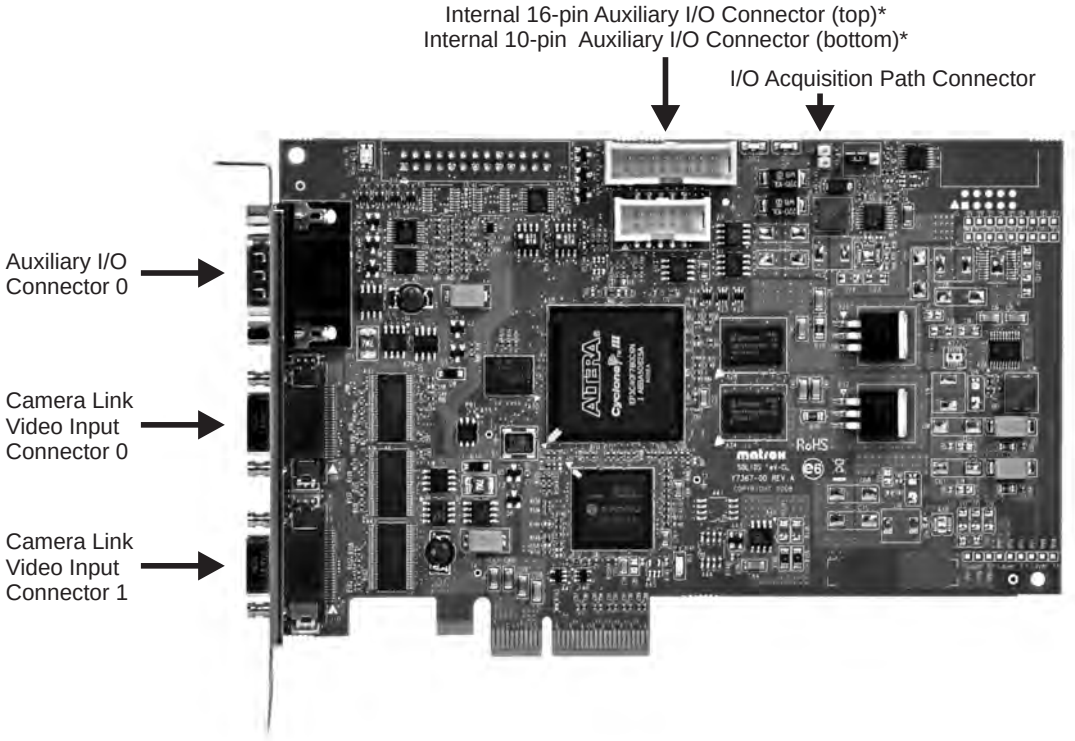
Dimensions and environmental specifications

The following dimensions and environmental specifications apply to all Matrox Solios eV-CL boards:

- Dimensions: 16.76 L x 11.12 H x 1.56 W cm (6.6" x 4.376" x 0.613") from bottom edge of goldfinger to top edge of board.
- Ventilation: 100 LFM between boards.
- Minimum/maximum ambient operating temperature: 0°C to55°C (32°F to 131°F).
- Minimum/maximum storage temperature: -40°C to 75°C (-40°F to 167°F).
- Operating relative humidity: up to 95% relative humidity (non-condensing).
- Storage humidity: 0 to 95% relative humidity (non-condensing).

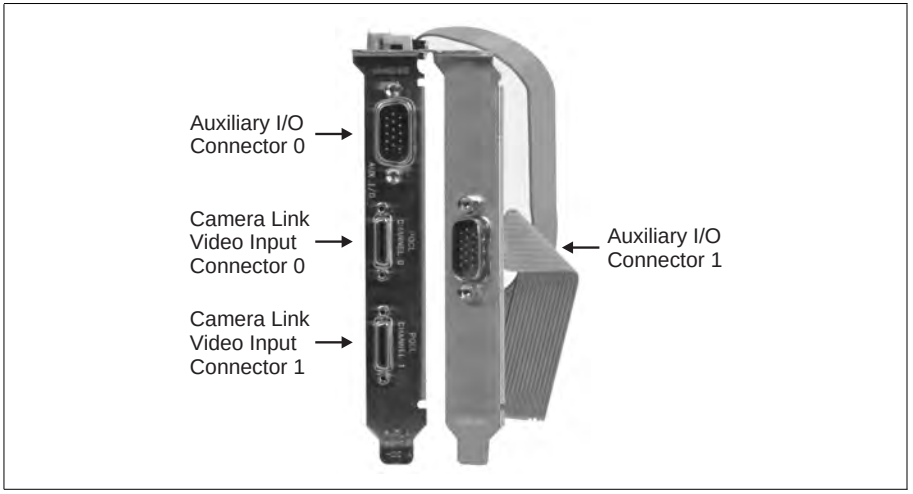
Connectors on Matrox Solios eV-CLB and eV-CLF boards

On the Matrox Solios eV-CLB and Matrox Solios eV-CLF boards, there are several interface connectors. On their bracket, there are two mini Camera Link video input connectors and an auxiliary I/O connector. In addition, close to the top edge of the boards, there are two internal auxiliary I/O connectors.



*Use the 16-pin auxiliary I/O connector to connect to the DB-15 cable adapter bracket; use the 10-pin auxiliary I/O connector to connect to the DB-9 cable adapter bracket.

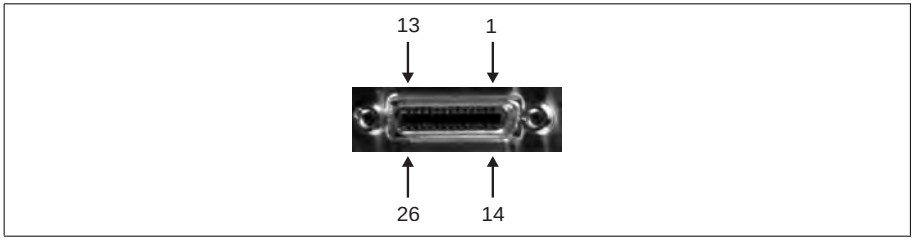
On the cable adapter bracket, there is another external auxiliary I/O connector (DB-15 or DB-9); this allow you to access the signals of the internal auxiliary I/O connectors from outside the computer enclosure.



❖ Note that the Matrox Solios eV-CL signal names have a ranking that reflects the number of signals of that type, format, and direction for a path. For example, two TTL and two LVDS auxiliary input signals for path 0 would be named P0_TTL_AUX_IN0, P0_TTL_AUX_IN1, P0_LVDS_AUX_IN0+, and P0_LVDS_AUX_IN1+. Notice that the ranking of the LVDS signals also starts at 0.

Camera Link video input connectors

On Matrox Solios eV-CLB and Matrox Solios eV-CLF, the two mini Camera Link video input connectors are 26-pin high-density female mini Camera Link connectors (HDR or SDR). The connectors are used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber. The pinout of these connectors follow the Camera Link standard.



For Matrox Solios eV-CLB in dual-Base configuration, the two Camera Link video input connectors have the same pinout; this pinout is listed in the following table. Note that, in dual-Base configuration, each connector supports video input from a different video source.

Pin	Signal	Description	Pin	Signal	Description
1	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.	14	Inner shield	Ground.
2	CC4-	Camera control output 4 (negative). See pin 15 for more information.	15	CC4+	Camera control output 4 (positive). Specific to the acq. path: exposure output from timer 1 or 2; user-defined output M_CC0 or M_CC1.
3	CC3+	Camera control output 3 (positive). Specific to the acq. path: exposure output from timer 1 or 2; user-defined output M_CC0 or M_CC1.	16	CC3-	Camera control output 3 (negative). See pin 3 for more information.
4	CC2-	Camera control output 2 (negative). See pin 17 for more information.	17	CC2+	Camera control output 2 (positive). Specific to the acq. path: exposure output from timer 1 or 2; user-defined output M_CC0 or M_CC1.
5	CC1+	Camera control output 1 (positive). Specific to the acq. path: exposure output from timer 1 or 2; user-defined output M_CC0 or M_CC1.	18	CC1-	Camera control output 1 (negative). See pin 5 for more information.
6	SerTFG+	Serial port to frame grabber (UART) (positive).	19	SerTFG-	Serial port to frame grabber (UART) (negative).
7	SerTC-	Serial port to video source (UART) (negative).	20	SerTC+	Serial port to video source (UART) (positive).
8	X3+	Video input data X3 (positive).	21	X3-	Video input data X3 (negative).
9	Xclk+	Clock input X (positive).	22	Xclk-	Clock input X (negative).
10	X2+	Video input data X2 (positive).	23	X2-	Video input data X2 (negative).
11	X1+	Video input data X1 (positive).	24	X1-	Video input data X1 (negative).
12	X0+	Video input data X0 (positive).	25	X0-	Video input data X0 (negative).
13	Inner shield	Ground.	26	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.

For Matrox Solios eV-CLB in single-Medium configuration and Matrox Solios eV-CLF, the first connector has the pinout described above, while the second connector has the following pinout.

Pin	Signal	Description	Pin	Signal	Description
1	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.	14	Inner shield	Ground.
2	Z3+	Video input data Z3 (positive).*	15	Z3-	Video input data Z3 (negative).*
3	Zclk+	Clock input Z (positive).*	16	Zclk-	Clock input Z (negative).*
4	Z2+	Video input data Z2(positive).*	17	Z2-	Video input data Z2 (negative).*
5	Z1+	Video input data Z1 (positive).*	18	Z1-	Video input data Z1 (negative).*
6	Z0+	Video input data Z0 (positive).*	19	Z0-	Video input data Z0 (negative).*
7	terminated	Unused.*	20	100 Ω	Unused.*
8	Y3+	Video input data Y3 (positive).	21	Y3-	Video input data Y3 (negative).
9	Yclk+	Clock input Y (positive).	22	Yclk-	Clock input Y (negative).
10	Y2+	Video input data Y2 (positive).	23	Y2-	Video input data Y2 (negative).
11	Y1+	Video input data Y1 (positive).	24	Y1-	Video input data Y1 (negative).
12	Y0+	Video input data Y0 (positive).	25	Y0-	Video input data Y0 (negative).
13	Inner shield	Ground.	26	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.

*. When the board is configured in single-Medium mode, these pins are reserved.

To interface with the above connectors, use a standard Camera Link cable with a 26-pin high-density male mini Camera Link connector (HDR or SDR) at one end. You can purchase such a cable from your video source manufacturer, Components Express inc., 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties. Note that this cable is not available from Matrox.

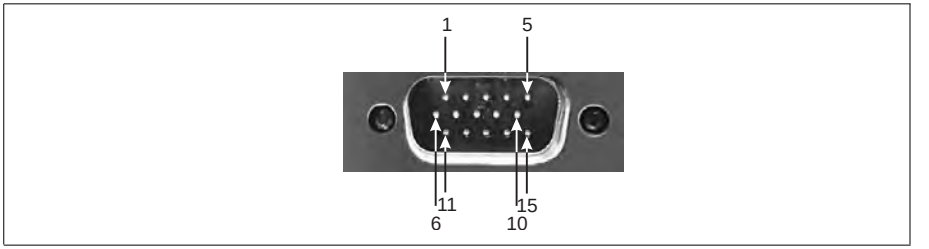
❖ If using both Camera Link connectors to connect to the same video source (single-Medium mode or single-Full mode), the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

External auxiliary I/O connector 0

External auxiliary I/O connector 0 on the Matrox Solios eV-CLB and Matrox Solios eV-CLF bracket is a high-density DB-15 male connector. It is used to transmit/receive auxiliary signals for one of the acquisition paths. By default, it carries the auxiliary signals for acquisition path 0; if a jumper is installed on the 2-pin I/O acquisition path connector, the auxiliary I/O connector carries the auxiliary signals for acquisition path 1.

❖ The auxiliary I/O connector on Matrox Solios eV-CLB and Matrox Solios eV-CLF is not compatible with display devices. Connecting the DB-15 connector on Matrox Solios eV-CLB or Matrox Solios eV-CLF to a VGA monitor or any other display device might damage both the device and the board.

The pinout for the auxiliary I/O connector is as follows. TC stands for trigger controller and acq. path stands for acquisition path. If the auxiliary signal is specific to an acquisition path, it is received/generated by the PSG of that path. If the auxiliary signal is not specific to an acquisition path, either PSG can typically receive/generate the auxiliary signal; if there is a functionality that can only be received/generated by a specific PSG, its acquisition path is indicated.



Pin	Signal	Description
1	P0_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 0. Supported signals: exposure output from timer 3, trigger input to TC0 (M_HARDWARE_PORT8), field polarity input, or user-defined input/output 2.
2	P0_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 0. Supported signals: exposure output from timer 1 or 4, trigger input to TC1 (M_HARDWARE_PORT9), or user-defined input/output 3.
3	TTL_AUX_IO_0	TTL auxiliary input/output 0 for an unspecified acq. path. Supported signals: exposure output from timer 2 of acq. path 0 only, trigger input to TC2 (M_HARDWARE_PORT2), or user-defined input/output 4,
4	P0_LVDS_AUX_IN0+	LVDS auxiliary input 0 for acq. path 0 (positive). Supported signals: trigger input to TC0 (M_HARDWARE_PORT10), field polarity input, user-defined input 10, or quadrature input bit 0.

Pin	Signal	Description
5	P0_LVDS_AUX_IN0-	LVDS auxiliary input 0 for acq. path 0 (negative). See pin 4 for more information.
6	P0_LVDS_AUX_IN1+	LVDS auxiliary input 1 for acq. path 0 (positive). Supported signals: trigger input to TC1 (M_HARDWARE_PORT11), timer-clock input 0, user-defined input 11, or quadrature input bit 1.
7	GND	Ground.
8.	P0_LVDS_AUX_IN1-	LVDS auxiliary input 1 for acq. path 0 (negative). See pin 6 for more information.
9	P0_OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for acq. path 0 (negative). See pin 15 for more information.
10	GND	Ground.
11	P0_OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for acq. path 0 (negative). See pin 12 for more information.
12	P0_OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 (positive). Supported signals: trigger input to TC1 (M_HARDWARE_PORT7), or user-defined input 13.
13	P0_LVDS_AUX_OUT0+	LVDS auxiliary output for acq. path 0 (positive). Supported signals: exposure output from timer 1, or user-defined output 0.
14	P0_LVDS_AUX_OUT0-	LVDS auxiliary output for acq. path 0 (negative). See pin 13 for more information.
15	P0_OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for acq. path 0 (positive). Supported signals: trigger input to TC0 (M_HARDWARE_PORT6), field polarity input, user-defined input 12.
-	NC	Not connected.

To build your own cable, you can purchase the following parts:

	Mating information
Manufacturer:	NorComp, Inc.
Connector:	180-015-203L001
Backshell:	970-015-010-011

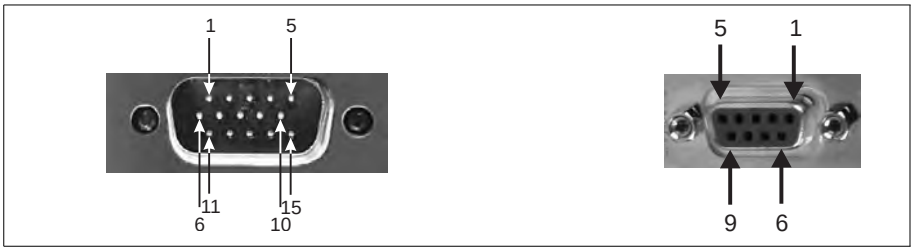
These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 1 on cable adapter bracket

External auxiliary I/O connector 1 on the Matrox Solios eV-CLB and Matrox Solios eV-CLF cable adapter bracket is a high-density DB-15 male or DB-9[1] female connector. It is used to transmit/receive auxiliary signals for one of the acquisition paths. By default, it carries the auxiliary signals for acquisition path 1; if a jumper is installed on the 2-pin I/O acquisition path connector, the auxiliary I/O connector carries the auxiliary signals for acquisition path 0.

❖ The DB-15 auxiliary I/O connector on the bracket is not compatible with display devices. Connecting the DB-15 connector on the bracket to a VGA monitor or any other display device might damage both the device and the board.

The pinout for the auxiliary I/O connector is as follows. TC stands for trigger controller and acq. path stands for acquisition path. If the auxiliary signal is specific to an acquisition path, it is received/generated by the PSG of that path. If the auxiliary signal is not specific to an acquisition path, either PSG can typically receive/generate the auxiliary signal; if there is a functionality that can only be received/generated by a specific PSG, its acquisition path is indicated.



Pin on DB-15	Pin on DB-9	Signal	Description
1	1	P1_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 1. Supported signals: exposure output from timer 3, trigger input to TC0 (M_HARDWARE_PORT8), field polarity input, or user-defined input/output 2.

1. If you purchase the SOLEVAACC01PAK* accessory kit, you obtain the cable adapter bracket with the DB-9 connector. In this case, the DB-9 connector has the same pinout as auxiliary I/O connector 1 (DB-9) on the adapter board of other Matrox Solios eCL/XCL boards. Note however, when using the optional DB-9 connector, some DB-15 signals are not available.

Pin on DB-15	Pin on DB-9	Signal	Description
2	-	P1_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 1. Supported signals: exposure output from timer 1 or 4, trigger input to TC1 (M_HARDWARE_PORT9), or user-defined input/output 3.
3	-	TTL_AUX_IO_1	TTL auxiliary input/output 1 for an unspecified acq. path. Supported signals: exposure output from timer 2 of acq. path 1 only, trigger input to TC3 (M_HARDWARE_PORT3), or user-defined input/output 5,
4	8	LVDS_AUX_IN0+	LVDS auxiliary input 0 for an unspecified acq. path (positive). Supported signals: trigger input to TC2 of acq. path 0 or TC0 or TC2 of acq. path 1 (M_HARDWARE_PORT4), field polarity input, user-defined input 6, or quadrature input bit 0.
5	3	LVDS_AUX_IN0-	LVDS auxiliary input 0 for an unspecified acq. path (negative). See pin 4 for more information.
6	-	LVDS_AUX_IN1+	LVDS auxiliary input 1 for an unspecified acq. path (positive). Supported signals: trigger input to TC3 of acq. path 0 or TC1 or TC3 of acq. path 1 (M_HARDWARE_PORT5), timer-clock input 0, user-defined input 7, or quadrature input bit 1.
7	6	GND	Ground.
8.	-	LVDS_AUX_IN1-	LVDS auxiliary input 1 for an unspecified acq. path (negative). See pin 6 for more information.
9	2	OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for an unspecified acq. path (negative). See pin 15 for more information.
10	-	GND	Ground.
11	5	OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for an unspecified acq. path (negative). See pin 12 for more information.
12	4	OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for an unspecified acq. path (positive). Supported signals: trigger input to TC3 of acq. path 0 or TC1 or TC3 of acq. path 1 (M_HARDWARE_PORT1), or user-defined input 9.
13	-	P1_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 1 (positive). Supported signals: exposure output from timer 1, or user-defined output 0.
14	-	P1_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 1 (negative). See pin 13 for more information.
15	7	OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for an unspecified acq. path (positive). Supported signals: trigger input to TC2 of acq. path 0 or TC0 or TC2 of acq. path 1 (M_HARDWARE_PORT0), field polarity input, user-defined input 8.
-	9	NC	Not connected.

To build your own cable, you can purchase the following parts:

	Mating information for DB-15	Mating information for DB-9
Manufacturer:	NorComp, Inc.	NorComp, Inc.
Connector:	180-015-203L001	172-E09-102-031
Backshell:	970-015-010-011	970-009-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

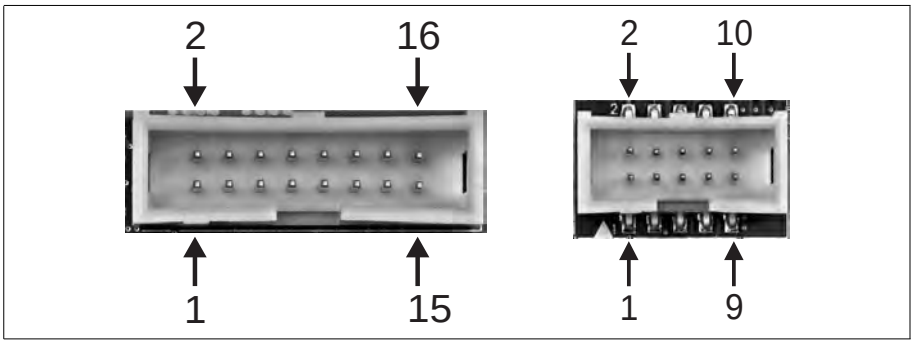
Internal 16-pin auxiliary I/O connector (top) and 10-pin auxiliary I/O connector (bottom)

The internal 16-pin auxiliary I/O connector (top) and the internal 10-pin auxiliary I/O connector (bottom) on the Matrox Solios eV-CLB and Matrox Solios eV-CLF boards are 0.1" spacing, 16-pin and 10-pin male connectors, respectively. You can use one of the connectors to transmit/receive auxiliary signals for one of the acquisition paths. By default, the auxiliary I/O connectors carry the auxiliary signals for acquisition path 1; if a jumper is installed on the 2-pin I/O acquisition path connector, the auxiliary I/O connectors carry the auxiliary signals for acquisition path 0. The connectors are located close to the top edge of the board, making the auxiliary signals accessible from inside the computer enclosure.

Warning

❖ The internal 16-signal auxiliary I/O connector and the internal 10-signal auxiliary I/O connector are mutually exclusive. You can use one or the other, but not both.

The pinout for these connectors are as follows. Refer to the description of external auxiliary I/O connector 1 to establish if an auxiliary signal is specific to an independent acquisition path and the type of signals that can be routed onto it.



Pin on 16-pin connector	Pin on 10-pin connector	Signal	Signal if jumper is installed
1	5	LVDS_AUX_IN0-	P0_TTL_AUX_IO_0
2	6	LVDS_AUX_IN0+	P0_TTL_AUX_IO_1
3	4	OPTO_AUX_IN0+	TTL_AUX_IO_0
4	2	GND	P0_LVDS_AUX_IN0+
5	-	TTL_AUX_IO_1	P0_LVDS_AUX_IN0-
6	3	OPTO_AUX_IN0-	P0_LVDS_AUX_IN1+
7	-	P1_LVDS_AUX_OUT0-	GND
8	-	P1_LVDS_AUX_OUT0+	P0_LVDS_AUX_IN1-
9.	-	LVDS_AUX_IN1-	P0_OPTO_AUX_IN0-
10	-	LVDS_AUX_IN1+	GND
11	-	P1_TTL_AUX_IO_1	P0_OPTO_AUX_IN1-
12	-	GND	P0_OPTO_AUX_IN1+
13	1	P1_TTL_AUX_IO_0	P0_LVDS_AUX_OUT0+
14	7	OPTO_AUX_IN1+	P0_LVDS_AUX_OUT0-
15	9	OPTO_AUX_IN1-	P0_OPTO_AUX_IN0+
16	-	NC	NC

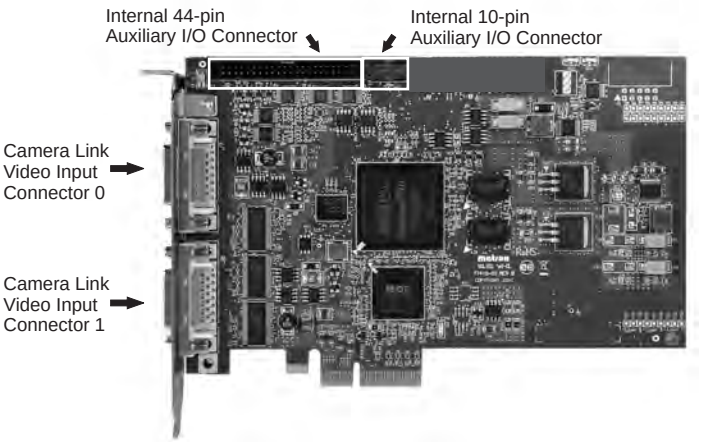
Internal I/O acquisition path jumper block

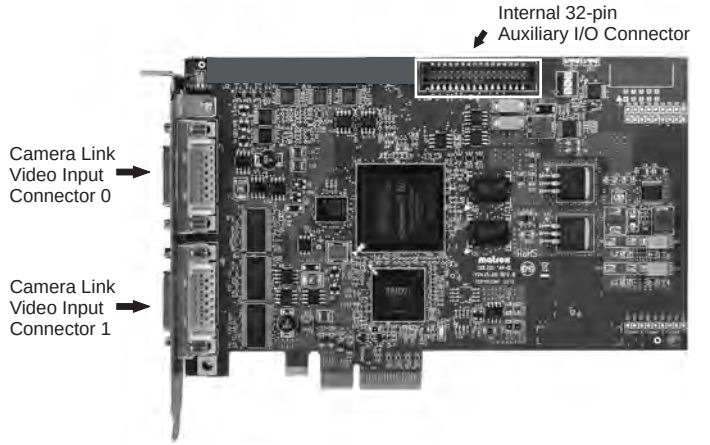
The internal I/O acquisition path jumper block is a 0.1" spacing, 2-pin connector. It is used to establish if auxiliary I/O connector 0 and auxiliary I/O connector 1 swap their pinout description.

Jumper	Description
Not installed (default)	Auxiliary I/O connector 0 has the pinout description which includes P0_... signals. Auxiliary I/O connector 1 has the pinout description which includes P1_... signals.
Installed	Auxiliary I/O connector 0 has the pinout description which includes P1_... signals. Auxiliary I/O connector 1 has the pinout description which includes P0_... signals.

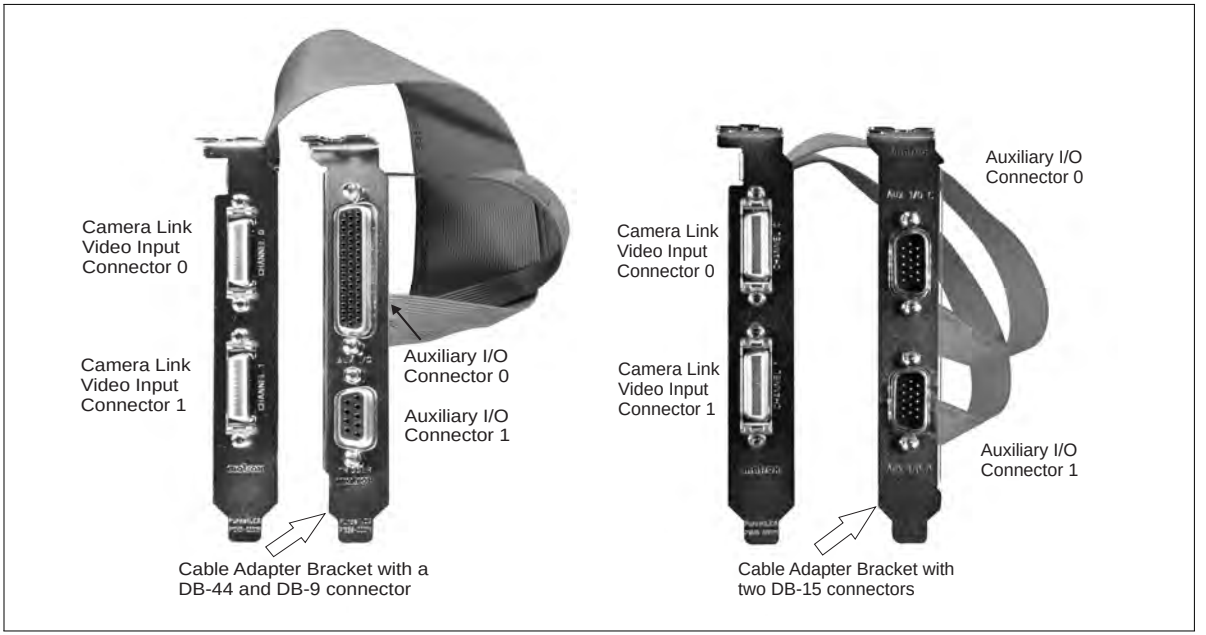
Connectors on Matrox Solios eV-CLBL and Matrox Solios eV-CLFL boards

On the Matrox Solios eV-CLBL and the Matrox Solios eV-CLFL boards, there are several interface connectors. On their bracket, there are two Camera Link video input connectors. In addition, depending on the cable adapter bracket received, there is either a 44-pin and 10-pin set of internal auxiliary I/O connectors for use with the DB-44/DB-9 external auxiliary I/O connectors, or there is a 32-pin internal auxiliary I/O connector for use with the dual DB-15 external auxiliary I/O connectors, as shown in the following two images.





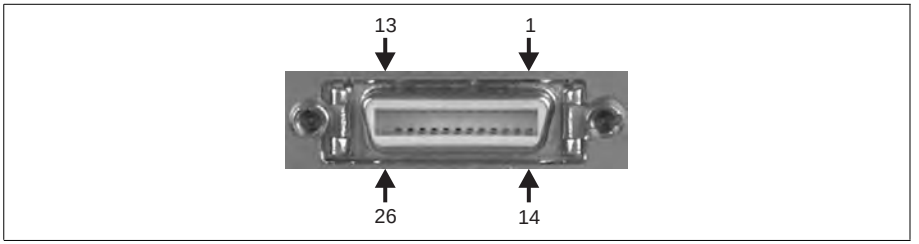
On the cable adapter bracket, there are two external auxiliary I/O connectors; these allow you to access the signals of the internal auxiliary I/O connectors from outside the computer enclosure. Depending on the board you selected, there are two cable adapter brackets available: one with a DB-44 and a DB-9 connector, and one with two DB-15 connectors.



❖ Note that the Matrox Solios eV-CL signal names have a ranking that reflects the number of signals of that type, format, and direction for a path. For example, two TTL and two LVDS auxiliary input signals for path 0 would be named P0_TTL_AUX_IN0, P0_TTL_AUX_IN1, P0_LVDS_AUX_IN0+, and P0_LVDS_AUX_IN1+. Notice that the ranking of the LVDS signals also starts at 0.

Camera Link video input connectors

On Matrox Solios eV-CLBL and Matrox Solios eV-CLFL, the two Camera Link video input connectors are 26-pin high-density female Camera Link connectors (MDR). The connectors are used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.



The pinout of these connectors follow the Camera Link standard, and are identical to the pinout of the corresponding connectors on Matrox Solios eV-CLB and Matrox Solios eV-CLF described earlier in this appendix.

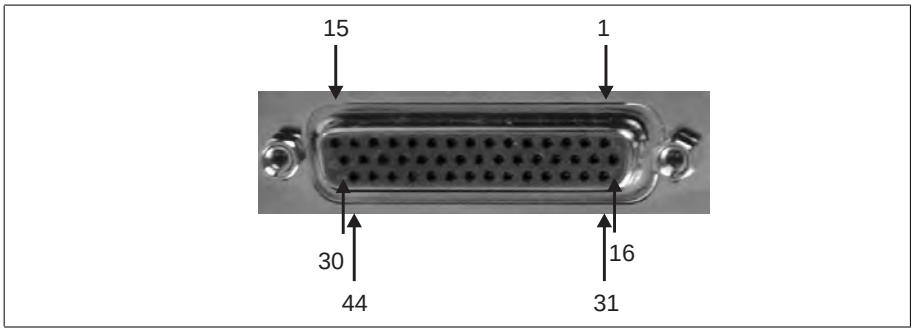
To interface with the above connectors, use a standard Camera Link cable with a 26-pin high-density male Camera Link connector (MDR) at one end. You can purchase such a cable from your video source manufacturer, Components Express inc., 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties. Note that this cable is not available from Matrox.

❖ If using both Camera Link connectors to connect to the same video source (single-Medium mode or single-Full mode), the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

External auxiliary I/O connector 0 on the DB-44/DB-9 cable adapter bracket

External auxiliary I/O connector 0 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL DB-44/DB-9 cable adapter bracket is a high-density DB-44 female connector. It is used to transmit timing and synchronization signals, and transmit/receive auxiliary signals. It interfaces with the 44-pin internal auxiliary I/O connector on the board, making the I/O signals accessible outside the computer enclosure.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an independent acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	P1_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 1. Supported signals: exposure output from timer 1 or 4, trigger input to TC1 (M_HARDWARE_PORT9), or user-defined input/output 3.
2	P1_LVDS_AUX_OUT1+	LVDS auxiliary output for acq. path 1 (positive). Supported signals: exposure output from timer 2, or user-defined output 1.
3	P0_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 0 (negative). See pin 19 for more information.
4	P0_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 0 (negative). See pin 20 for more information.
5	P1_LVDS_HSYNC_OUT-	HSYNC output for acq. path 1 (negative). See pin 6 for more information.
6	P1_LVDS_HSYNC_OUT+	HSYNC output for acq. path 1 (positive).
7	P1_LVDS_CLK_OUT+	Clock output for acq. path 1 (positive).
8	OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for an unspecified acq. path (negative). See pin 24 for more information.
9	NC	Not connected.
10	NC	Not connected.
11	P0_LVDS_CLK_OUT+	Clock output for acq. path 0 (positive).
12	LVDS_AUX_IN1+	LVDS auxiliary input 1 for an unspecified acq. path (positive). Supported signals: trigger input to TC3 of acq. path 0 or TC1 or TC3 of acq. path 1 (M_HARDWARE_PORT5), timer-clock input 0, user-defined input 7, or quadrature input bit 1.
13	P0_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 0. Supported signals: exposure output from timer 1 or 4, trigger input to TC1 (M_HARDWARE_PORT9), or user-defined input/output 3.
14	GND	Ground.
15	TTL_AUX_IO_1	TTL auxiliary input/output 1 for an unspecified acq. path. Supported signals: exposure output from timer 2 of acq. path 1 only, trigger input to TC3 (M_HARDWARE_PORT3), or user-defined input/output 5,.
16	GND	Ground.
17	P1_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 1 (negative). See pin 2 for more information.
18	P1_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 1 (negative). See pin 33 for more information.
19	P0_LVDS_AUX_OUT1+	LVDS auxiliary output for acq. path 0 (positive). Supported signals: exposure output from timer 2, or user-defined output 1.

Pin	Signal	Description
20	P0_LVDS_AUX_OUT0+	LVDS auxiliary output for acq. path 0 (positive). Supported signals: exposure output from timer 1, or user-defined output 0.
21	P1_LVDS_VSYNC_OUT-	VSYNC output for acq. path 1 (negative). See pin 36 for more information.
22	P1_LVDS_CLK_OUT-	Clock output for acq. path 1 (negative). See pin 7 for more information.
23	P0_LVDS_AUX_IN1-	LVDS auxiliary input 1 for acq. path 0 (negative). See pin 37 for more information.
24	OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for an unspecified acq. path (positive). Supported signals: trigger input to TC2 of acq. path 0 or TC0 or TC2 of acq. path 1 (M_HARDWARE_PORT0), field polarity input, user-defined input 8.
25	P0_LVDS_VSYNC_OUT-	VSYNC output for acq. path 0 (negative). See pin 40 for more information.
26	P0_LVDS_HSYNC_OUT-	HSYNC output for acq. path 0 (negative). See pin 41 for more information.
27	P0_LVDS_CLK_OUT-	Clock output for acq. path 0 (negative). See pin 11 for more information.
28	LVDS_AUX_IN1-	LVDS auxiliary input 1 for an unspecified acq. path (negative). See pin 12 for more information.
29	GND	Ground.
30	GND	Ground.
31	LVDS_AUX_IN0-	LVDS auxiliary input 0 for an unspecified acq. path (negative). See pin 32 for more information.
32	LVDS_AUX_IN0+	LVDS auxiliary input 0 for an unspecified acq. path (positive). Supported signals: trigger input to TC2 of acq. path 0 or TC0 or TC2 of acq. path 1 (M_HARDWARE_PORT4), field polarity input, user-defined input 6, or quadrature input bit 0.
33	P1_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 1 (positive). Supported signals: exposure output from timer 1, or user-defined output 0.
34	GND	Ground.
35	P1_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 1. Supported signals: exposure output from timer 3, trigger input to TC0 (M_HARDWARE_PORT8), field polarity input, or user-defined input/output 2.
36	P1_LVDS_VSYNC_OUT+	VSYNC output for acq. path 1 (positive).
37	P0_LVDS_AUX_IN1+	LVDS auxiliary input 1 for acq. path 0 (positive). Supported signals: trigger input to TC1 (M_HARDWARE_PORT11), timer-clock input 0, user-defined input 11, or quadrature input bit 1.

Pin	Signal	Description
38	OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for an unspecified acq. path (positive). Supported signals: trigger input to TC3 of acq. path 0 or TC1 or TC3 of acq. path 1 (M_HARDWARE_PORT1), or user-defined input 9.
39	OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for an unspecified acq. path (negative). See pin 38 for more information.
40	P0_LVDS_VSYNC_OUT+	VSYNC output for acq. path 0 (positive).
41	P0_LVDS_HSYNC_OUT+	HSYNC output for acq. path 0 (positive).
42	GND	Ground.
43	TTL_AUX_IO_0	TTL auxiliary input/output 0 for an unspecified acq. path. Supported signals: exposure output from timer 2 of acq. path 0 only, trigger input to TC2 (M_HARDWARE_PORT2), or user-defined input/output 4,
44	NC	Not connected.

To build your own cable, you can purchase the following parts:

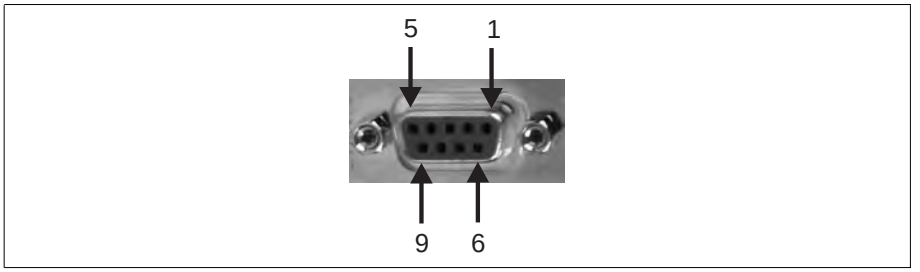
	Mating information
Manufacturer:	NorComp, Inc.
Connector:	180-044-102-001
Backshell:	970-025-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 1 on the DB-44/DB-9 cable adapter bracket

External auxiliary I/O connector 1 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL DB-44/DB-9 cable adapter bracket is a standard DB-9 female connector. It is used to transmit/receive auxiliary signals. It interfaces with the 10-pin internal auxiliary I/O connector on the board, making the I/O signals accessible outside the computer enclosure.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an independent acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	P0_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 0. Supported signals: exposure output from timer 3, trigger input to TC0 (M_HARDWARE_PORT8), field polarity input, or user-defined input/output 2.
2	P0_OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for acq. path 0 (negative). See pin 7 for more information.
3	P0_LVDS_AUX_IN0-	LVDS auxiliary input 0 for acq. path 0 (negative). See pin 8 for more information.
4	P0_OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 (positive). Supported signals: trigger input to TC1 (M_HARDWARE_PORT7), or user-defined input 13.
5	P0_OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for acq. path 0 (negative). See pin 4 for more information.
6	GND	Ground.
7	P0_OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for acq. path 0 (positive). Supported signals: trigger input to TC0 (M_HARDWARE_PORT6), field polarity input, user-defined input 12.
8	P0_LVDS_AUX_IN0+	LVDS auxiliary input 0 for acq. path 0 (positive). Supported signals: trigger input to TC0 (M_HARDWARE_PORT10), field polarity input, user-defined input 10, or quadrature input bit 0.
9	NC	Not connected.

To build your own cable, you can purchase the following parts:

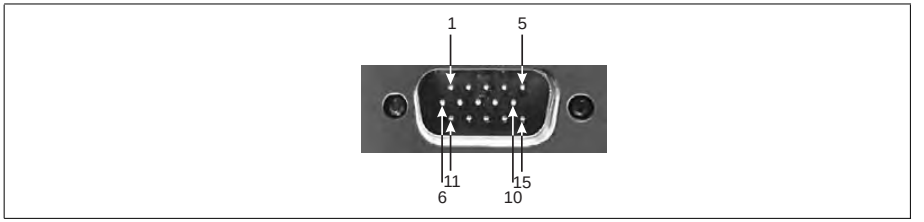
	Mating information
Manufacturer:	NorComp, Inc.
Connector:	172-E09-102-031
Backshell:	970-009-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 0 on the dual DB-15 cable adapter bracket

External auxiliary I/O connector 0 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL dual DB-15 cable adapter bracket is a high-density DB-15 male connector. It is used to transmit/receive auxiliary signals for acquisition path 0.

❖ Auxiliary I/O connector 0 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL dual DB-15 cable adapter bracket is not compatible with display devices. Connecting the DB-15 connector on the cable adapter bracket to a VGA monitor or any other display device might damage both the device and the board.



The pinout for external auxiliary I/O connector 0 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL dual DB-15 cable adapter bracket is identical to the pinout for external auxiliary I/O connector 0 on the Matrox Solios eV-CLB and Matrox Solios eV-CLF bracket; refer to that section for the pinout table.

To build your own cable, you can purchase the following parts:

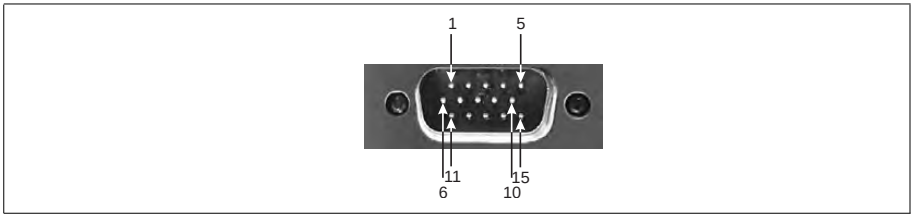
	Mating information
Manufacturer:	NorComp, Inc.
Connector:	180-015-203L001
Backshell:	970-015-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 1 on the dual DB-15 cable adapter bracket

External auxiliary I/O connector 1 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL dual DB-15 cable adapter bracket is a high-density DB-15 male connector. It is used to transmit/receive auxiliary signals for acquisition path 1.

❖ Auxiliary I/O connector 1 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL dual DB-15 cable adapter bracket is not compatible with display devices. Connecting the DB-15 connector on the cable adapter bracket to a VGA monitor or any other display device might damage both the device and the board.



The pinout for external auxiliary I/O connector 1 on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL dual DB-15 cable adapter bracket is identical to the pinout for external auxiliary I/O connector 1 on the Matrox Solios eV-CLB and Matrox Solios eV-CLF cable adapter bracket with a DB-15 connector; refer to that section for the pinout table.

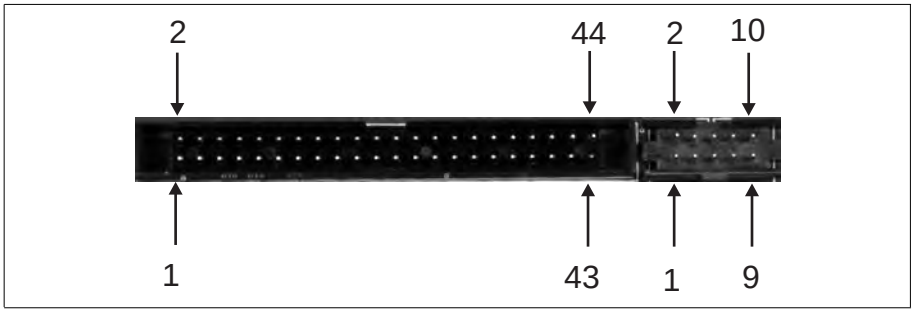
To build your own cable, you can purchase the following parts:

	Mating information for DB-15
Manufacturer:	NorComp, Inc.
Connector:	180-015-203L001
Backshell:	970-015-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

Internal 44-pin auxiliary I/O connector (left) and 10-pin auxiliary I/O connector (right)

The internal 44-pin auxiliary I/O connector (left) and the internal 10-pin auxiliary I/O connector (right) on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL board are 0.1" spacing, 44-pin and 10-pin male connectors, respectively. You can use the connectors to transmit/receive auxiliary signals for the two acquisition paths. The connectors are located close to the top edge of the board, making the auxiliary signals accessible from inside the computer enclosure.



The pinout for internal 44-pin auxiliary I/O connector is as follows. Refer to the description of external auxiliary I/O connector 1 to establish if an auxiliary signal is specific to an independent acquisition path and the type of signals that can be routed onto it.

Pin	Signal	Description
1	P1_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 1.
2	GND	Ground.
3	LVDS_AUX_IN0-	LVDS auxiliary input 0 for an unspecified acq. path (negative).
4	P1_LVDS_AUX_OUT1+	LVDS auxiliary output 1 for acq. path 1 (positive).
5	P1_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 1 (negative).
6	LVDS_AUX_IN0+	LVDS auxiliary input 0 for an unspecified acq. path (positive).
7	P0_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 0 (negative).
8	P1_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 1 (negative).
9	P1_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 1 (positive).
10	P0_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 0 (negative).
11	P0_LVDS_AUX_OUT1+	LVDS auxiliary output 1 for acq. path 0 (positive)
12	GND	Ground.
13	P1_LVDS_HSYNC_OUT-	HSYNC output for acq. path 1 (negative).
14	P0_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 0 (positive).
15	P1_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 1.
16	P1_LVDS_HSYNC_OUT+	HSYNC output for acq. path 1 (positive).
17	P1_LVDS_VSYNC_OUT-	VSYNC output for acq. path 1 (negative).
18	P1_LVDS_VSYNC_OUT+	VSYNC output for acq. path 1 (positive)
19	P1_LVDS_CLK_OUT+	Clock output for acq. path 1 (positive)
20	P1_LVDS_CLK_OUT-	Clock output for acq. path 1 (negative).
21	P0_LVDS_AUX_IN1+	LVDS auxiliary input 1 for acq. path 0 (positive).
22	OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for an unspecified acq. path (negative).
23	P0_LVDS_AUX_IN1-	LVDS auxiliary input 1 for acq. path 0 (negative).
24	OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for an unspecified acq. path (positive).
25	NC	Not connected.
26	OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for an unspecified acq. path (positive).
27	OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for an unspecified acq. path (negative).
28	NC	Not connected.
29	P0_LVDS_VSYNC_OUT-	VSYNC output for acq. path 0 (negative).

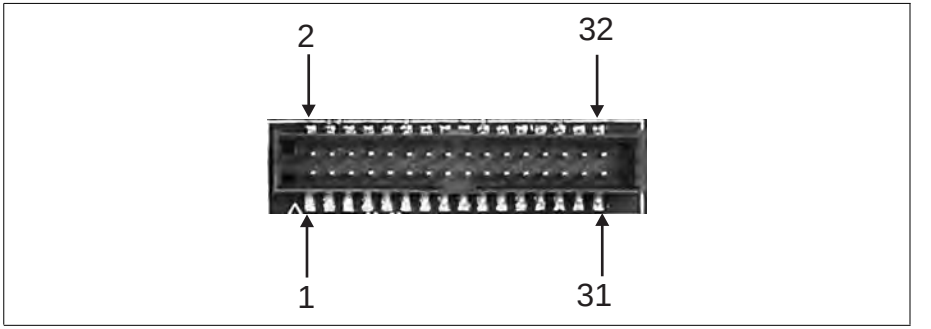
Pin	Signal	Description
30	P0_LVDS_VSYNC_OUT+	VSYNC output for acq. path 0 (positive).
31	P0_LVDS_CLK_OUT+	Clock output for acq. path 0 (positive).
32	P0_LVDS_HSYNC_OUT-	HSYNC output for acq. path 0 (negative).
33	P0_LVDS_HSYNC_OUT+	HSYNC output for acq. path 0 (positive).
34	LVDS_AUX_IN1+	LVDS auxiliary input 1 for an unspecified acq. path (positive).
35	P0_LVDS_CLK_OUT-	Clock output for acq. path 0 (negative).
36	GND	Ground.
37	P0_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 0.
38	LVDS_AUX_IN1-	LVDS auxiliary input 1 for an unspecified acq. path (negative).
39	TTL_AUX_IO_0	TTL auxiliary input/output 0 for an unspecified acq. path.
40	GND	Ground.
41	GND	Ground.
42	NC	Not connected.
43	TTL_AUX_IO_1	TTL auxiliary input/output 1 for an unspecified acq. path.
44	GND	Ground.

The pinout for internal 10-pin auxiliary I/O connector is as follows. Refer to the description of external auxiliary I/O connector 1 to establish if an auxiliary signal is specific to an independent acquisition path and the type of signals that can be routed onto it.

Pin	Signal	Description
1	P0_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 0.
2	GND	Ground.
3	P0_OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for acq. path 0 (negative).
4	P0_OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for acq. path 0 (positive).
5	P0_LVDS_AUX_IN0-	LVDS auxiliary input 0 for acq. path 0 (negative)
6	P0_LVDS_AUX_IN0+	LVDS auxiliary input 0 for acq. path 0 (positive).
7	P0_OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for acq. path 0 (positive).
8	NC	Not connected.
9	P0_OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for acq. path 0 (negative).
10	NC	Not connected.

Internal 32-pin auxiliary I/O connector

The internal 32-pin auxiliary I/O connector on the Matrox Solios eV-CLBL and Matrox Solios eV-CLFL board is a 0.1" spacing, 32-pin male connector. This connector is to be connected to the dual DB-15 connectors flat ribbon cable. You can use the connector to transmit/receive auxiliary signals for the two acquisition paths. The connector is located close to the top edge of the board, making the auxiliary signals accessible from inside the computer enclosure.



Pin	Signal	Description
1	P0_LVDS_AUX_IN0-	LVDS auxiliary input 0 for acq. path 0 (negative).
2	P0_LVDS_AUX_IN0+	LVDS auxiliary input 0 for acq. path 0 (positive).
3	P0_OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for acq. path 0 (positive).
4	GND	Ground.
5	TTL_AUX_IO_0	TTL auxiliary input/output 0 for an unspecified acq. path.
6	P0_OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for acq. path 0 (negative).
7	P0_LVDS_AUX_OUT0-	LVDS auxiliary output for acq. path 0 (negative).
8	P0_LVDS_AUX_OUT0+	LVDS auxiliary output for acq. path 0 (positive).
9	P0_LVDS_AUX_IN1-	LVDS auxiliary input 1 for acq. path 0 (negative).
10	P0_LVDS_AUX_IN1+	LVDS auxiliary input 1 for acq. path 0 (positive).
11	P0_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 0.
12	GND	Ground.
13	P0_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 0.
14	P0_OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 (positive).
15	P0_OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for acq. path 0 (negative).
16	NC	Not connected.
17	LVDS_AUX_IN0-	LVDS auxiliary input 0 for an unspecified acq. path (negative).

Pin	Signal	Description
18	LVDS_AUX_IN0+	LVDS auxiliary input 0 for an unspecified acq. path (positive).
19	OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for an unspecified acq. path (positive).
20	GND	Ground.
21	TTL_AUX_IO_1	TTL auxiliary input/output 1 for an unspecified acq. path.
22	OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for an unspecified acq. path (negative).
23	P1_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 1 (negative).
24	P1_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 1 (positive).
25	LVDS_AUX_IN1-	LVDS auxiliary input 1 for an unspecified acq. path (negative).
26	LVDS_AUX_IN1+	LVDS auxiliary input 1 for an unspecified acq. path (positive).
27	P1_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 1.
28	GND	Ground.
29	P1_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 1.
30	OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for an unspecified acq. path (positive).
31	OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for an unspecified acq. path (negative).
32	NC	Not connected.

Appendix C: Acknowledgments

This appendix lists the copyright information regarding third-party material used to implement components on the Matrox Solios eV-CL board.

UART copyright information

The following is the copyright notice for the UART design used on the Matrox Solios eV-CL boards.

Appendix D: Major revisions of Matrox Solios eV-CL boards

This appendix lists the major revisions of the Matrox Solios eV-CL boards.

Major revisions of Matrox Solios eV-CL

Versions of Matrox Solios eV-CL		
Part number	**Version**	**Description**
SOL2MEVCLB*	006	First shipping version.
SOL2MEVCLF*	006	First shipping version.

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Regulatory Compliance

FCC Compliance Statement

Warning

Changes or modifications to these units not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

The use of shielded cables for connections of these devices to other peripherals is required to meet the regulatory requirements.

Note

These devices comply with Part 15 of FCC Rules. Operation is subject to the following two conditions:

1. These devices may not cause harmful interference, and
2. These devices must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for Class A digital devices, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of these devices in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

Industry Canada Compliance Statement

These digital apparatuses do not exceed the Class A limits for radio noise emission from digital apparatuses set out in the Radio Interference Regulations of Industry Canada.

Ces appareils numériques n'émettent pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de Classe A prescrites dans le Règlement sur le brouillage radioélectrique édicté par Industrie Canada.

EU Notice (European Union)

WARNING: These are class A products. In a domestic environment these products may cause radio interference in which case the user may be required to take adequate measures.

AVERTISSEMENT: Ces appareils sont des produits informatiques de Classe A. Lorsque ces appareils sont utilisent dans un environnement résidentiel, ces produits peuvent entraîner des interférences radioélectriques. Dans ce cas, l'usager peut être prié de prendre des mesures correctives appropriées.

This device complies with EC Directive 89/336/EEC for Class A digital devices. They have been tested and found to comply with EN55022/CISPR22 and EN55024/CISPR24 when installed in a typical class A compliant host system. It is assumed that these devices will also achieve compliance in any Class A compliant system.

Ces unités sont conformes à la Directive communautaire 89/336/EEC pour les unités numériques de Classe A. Les tests effectués one prouvé qu'elles sont conformes aux normes EN55022/CISPR22 et EN55024/CISPR24 lorsqu'elles sont installées dans un système hôte typique de la Classe A. On suppose qu'ils présenteront la même compatibilité dans tout système compatible de la Classe A.

Directive on Waste Electrical and Electronic Equipment (WEEE)

Europe

(English) European user's information – Directive on Waste Electrical and Electronic Equipment (WEEE)

Please refer to the Matrox Web site (**www.matrox.com/environment/weee**) for recycling information.

(Français) Informations aux utilisateurs Européens – Règlementation des déchets d'équipements électriques et électroniques (DEEE)

Se référer au site Web de Matrox (**www.matrox.com/environment/weee**) pour l'information concernant le recyclage.

(Deutsch) Information für europäische Anwender – Europäische Regelungen zu Elektro- und Elektronikaltgeräten (WEEE)

Bitte wenden Sie sich an dem Matrox-Website (**www.matrox.com/environment/weee**) für Recycling Informationen.

(Italiano) Informazioni per gli utenti europei – Direttiva sui rifiuti di apparecchiature elettriche ed elettroniche (RAEE)

Si prega di riferirsi al sito Web Matrox (**www.matrox.com/environment/weee**) per le informazioni di riciclaggio.

Limited Warranty

Refer to the warranty statement that came with your product.